



PSMN1R2-30YLC

N-channel 30 V 1.25mΩ logic level MOSFET in LPAK using NextPower technology

Rev. 1 — 3 May 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, and QOSS for high system efficiencies at low and high loads
- Ultra low R_{ds(on)} and low parasitic inductance

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	[1] -	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	215	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; see Figure 12	-	1.35	1.65	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 12	-	1.05	1.25	mΩ



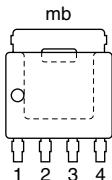
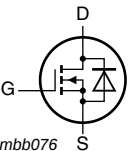
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; see Figure 14 ; see Figure 15	-	11.6	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; see Figure 14 ; see Figure 15	-	38	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK;
Power-SO8)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R2-30YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PSMN1R2-30YLC	1C230L

[1] % = placeholder for manufacturing site code

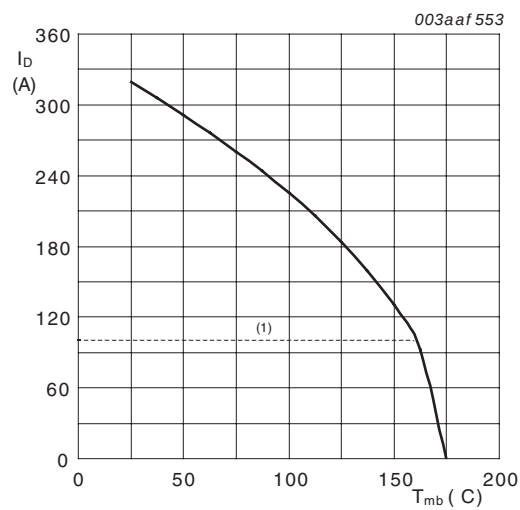
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

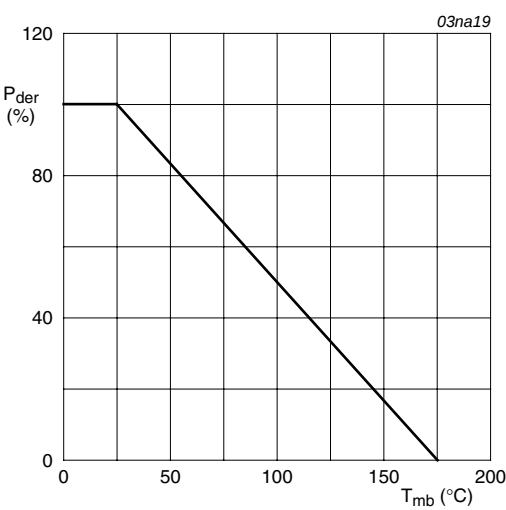
Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	30	V	
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	30	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	-	100	A
		V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	[1]	-	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 4	-	1237	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	215	W	
T _{stg}	storage temperature		-55	175	°C	
T _j	junction temperature		-55	175	°C	
T _{sld(M)}	peak soldering temperature		-	260	°C	
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	900	-	V	
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	1237	A	
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped; see Figure 3	-	209	mJ	

[1] Continuous current is limited by package.



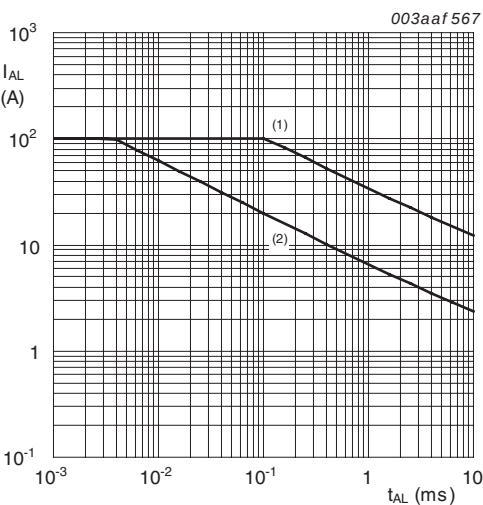
$V_{GS} \geq 10V$; (1) Capped at 100A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1) $T_{j (init)} = 25^{\circ}C$; (2) $T_{j (init)} = 100^{\circ}C$

Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

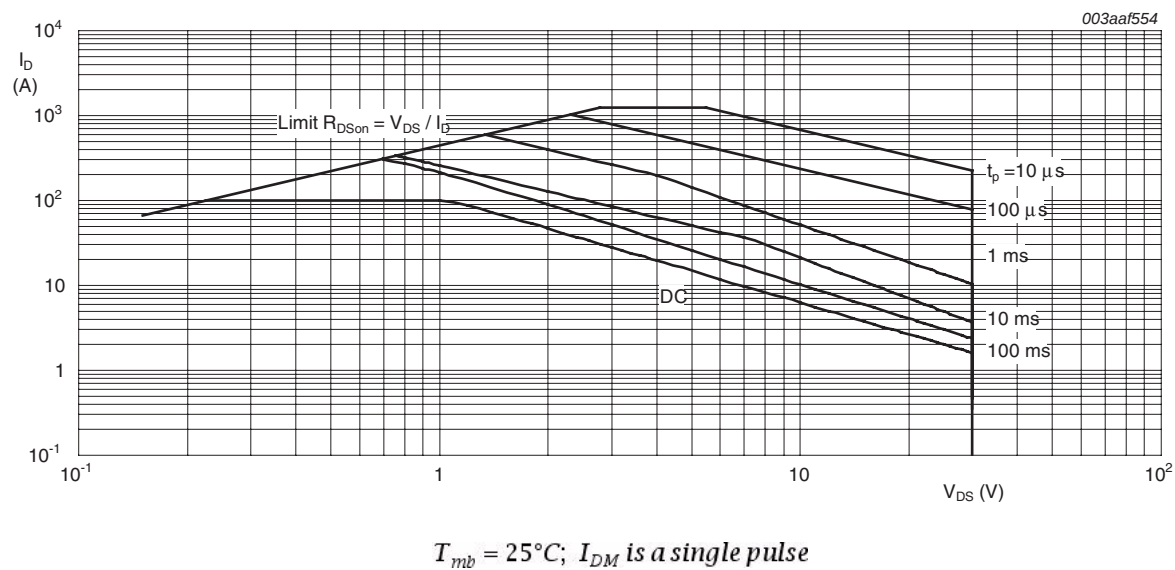


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.58	0.7	K/W

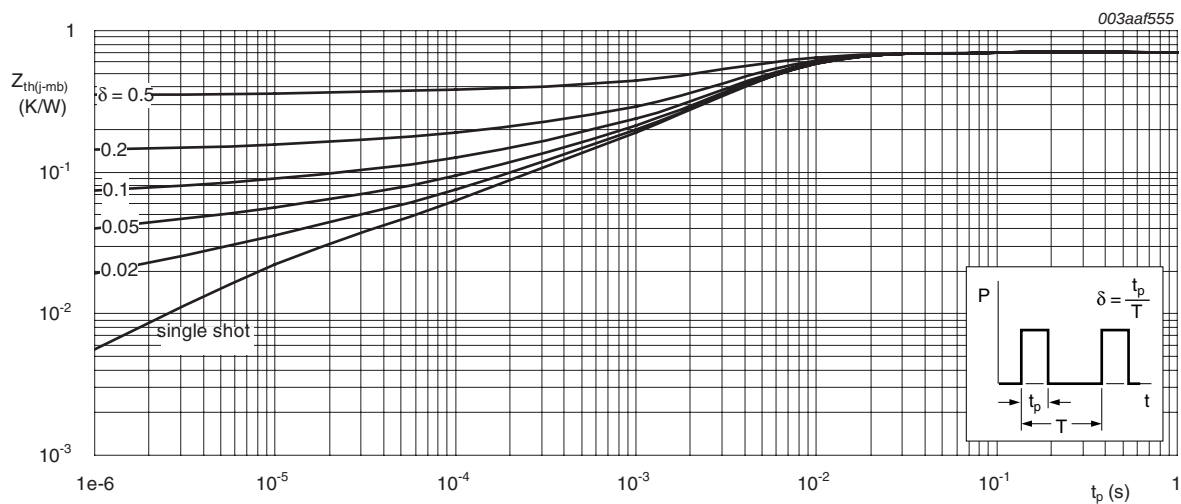


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$; see Figure 10 ; see Figure 11	1.05	1.46	1.95	V
		$I_D = 10\ mA$; $V_{DS} = V_{GS}$; $T_j = 150\ ^\circ C$	0.5	-	-	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ C$	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	1	μA
		$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_j = 150\ ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; see Figure 12	-	1.35	1.65	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_j = 150\ ^\circ C$; see Figure 13 ; see Figure 12	-	-	2.8	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; see Figure 12	-	1.05	1.25	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 150\ ^\circ C$; see Figure 13 ; see Figure 12	-	-	2.05	mΩ
R_G	gate resistance	$f = 1\ MHz$	-	1.1	2.2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ A$; $V_{DS} = 15\ V$; $V_{GS} = 10\ V$; see Figure 14 ; see Figure 15	-	78	-	nC
		$I_D = 25\ A$; $V_{DS} = 15\ V$; $V_{GS} = 4.5\ V$; see Figure 14 ; see Figure 15	-	38	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	75	-	nC
Q_{GS}	gate-source charge	$I_D = 25\ A$; $V_{DS} = 15\ V$; $V_{GS} = 4.5\ V$; see Figure 14 ; see Figure 15	-	10.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.6	-	nC
Q_{GD}	gate-drain charge		-	11.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ A$; $V_{DS} = 15\ V$; see Figure 14 ; see Figure 15	-	2.34	-	V
C_{iss}	input capacitance	$V_{DS} = 15\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_j = 25\ ^\circ C$; see Figure 16	-	5093	-	pF
C_{oss}	output capacitance		-	977	-	pF
C_{rss}	reverse transfer capacitance		-	333	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\ V$; $R_L = 0.6\ \Omega$; $V_{GS} = 4.5\ V$; $R_{G(ext)} = 4.7\ \Omega$	-	36	-	ns
t_r	rise time		-	60	-	ns
$t_{d(off)}$	turn-off delay time		-	75	-	ns
t_f	fall time		-	39	-	ns

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	33	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 17	-	0.8	1.1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	41.5	-	ns
Q_r	recovered charge	$V_{DS} = 15\text{ V}$	-	45	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}$; $I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{DS} = 15\text{ V}$; see Figure 18	-	25	-	ns
t_b	reverse recovery fall time		-	16.5	-	ns

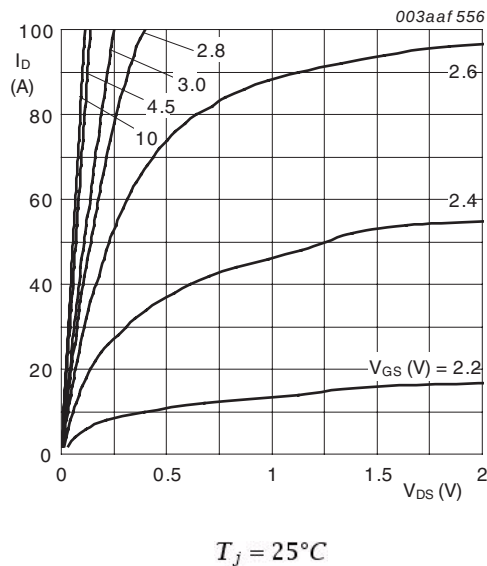


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

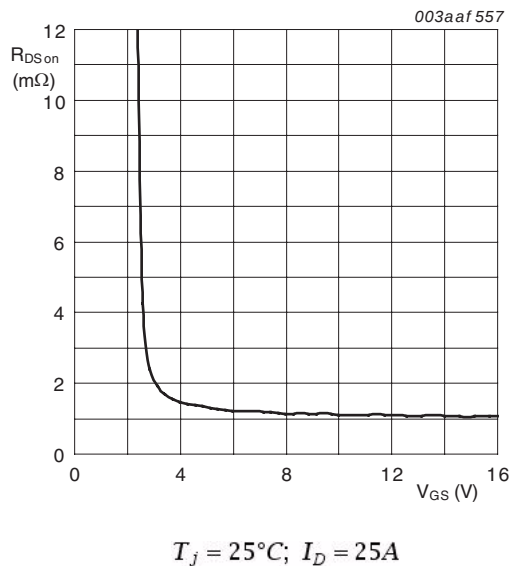


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

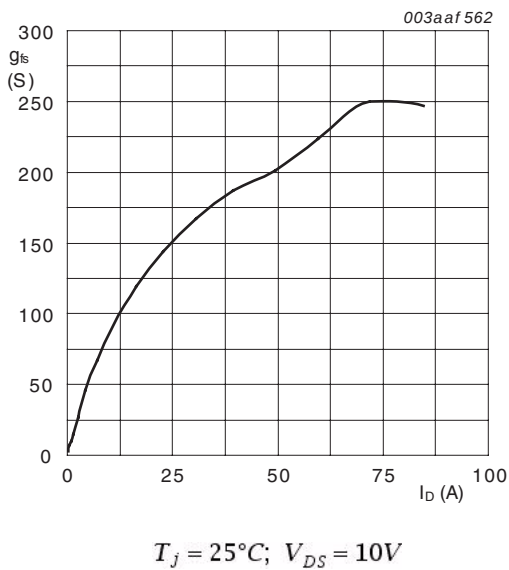


Fig 8. Forward transconductance as a function of drain current; typical values

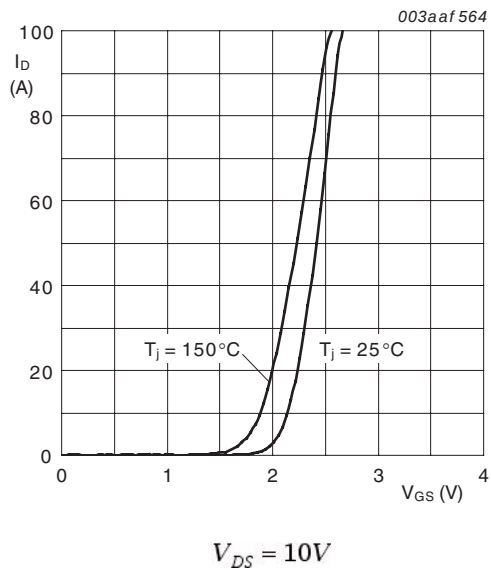


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage

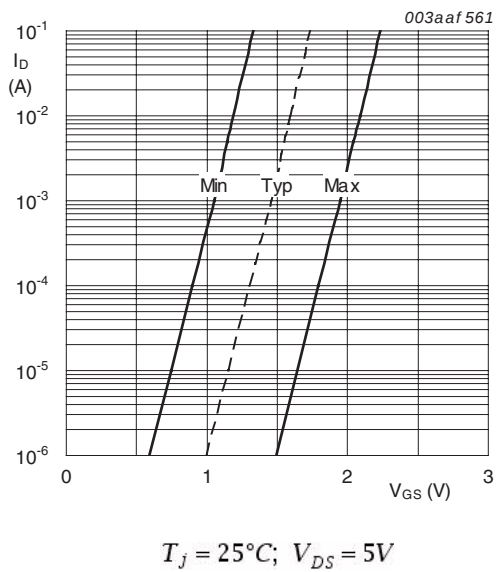


Fig 10. Sub-threshold drain current as a function of gate-source voltage

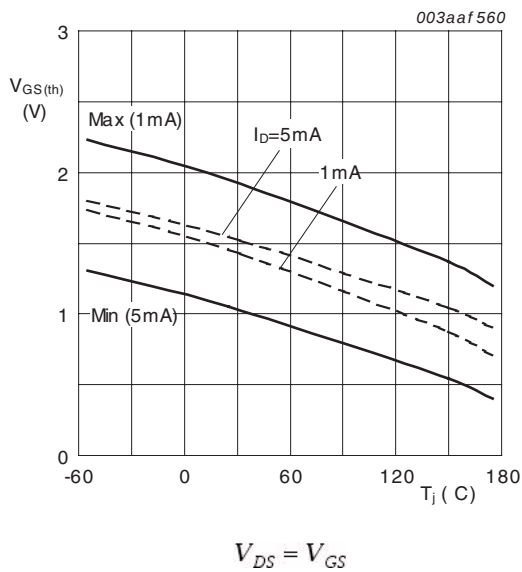


Fig 11. Gate-source threshold voltage as a function of junction temperature

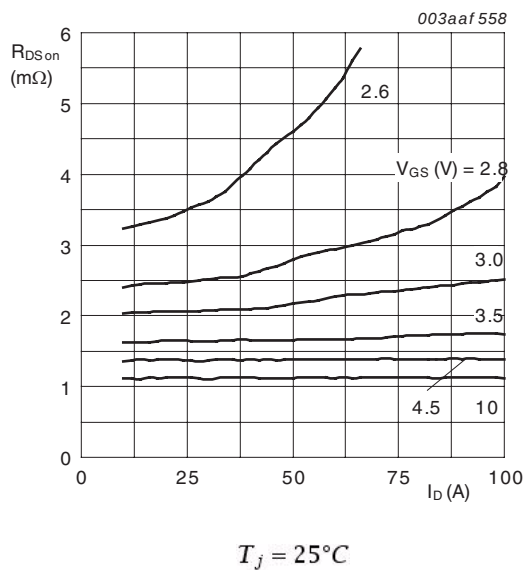


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

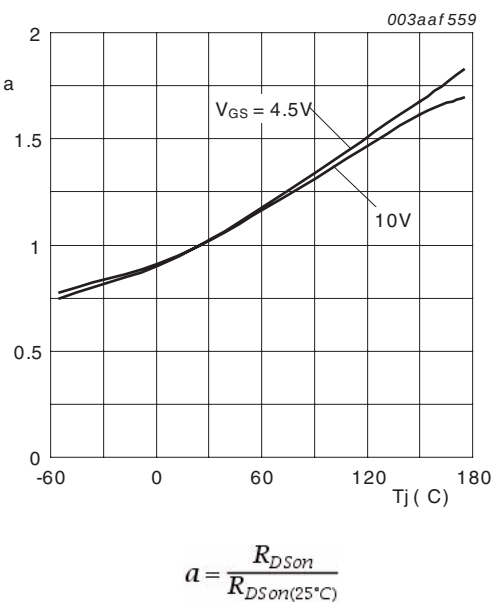


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

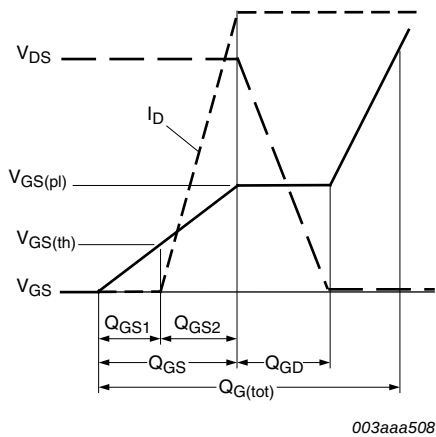


Fig 14. Gate charge waveform definitions

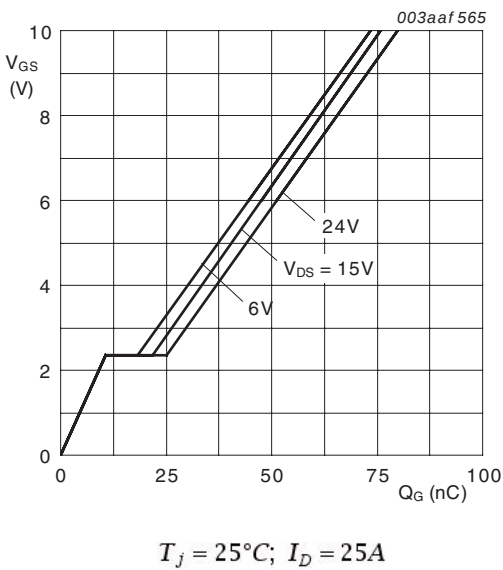


Fig 15. Gate-source voltage as a function of gate charge; typical values

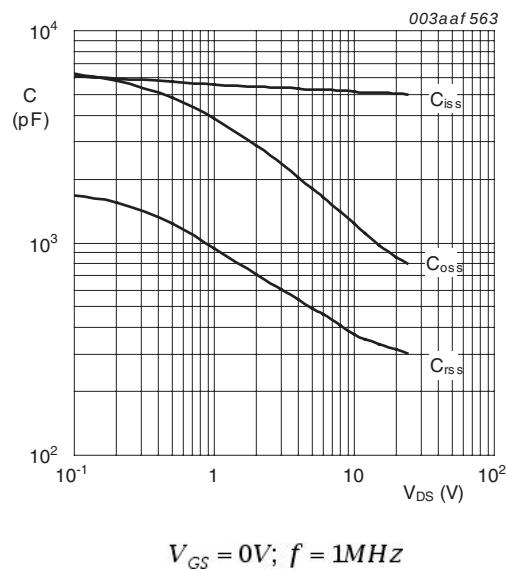


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

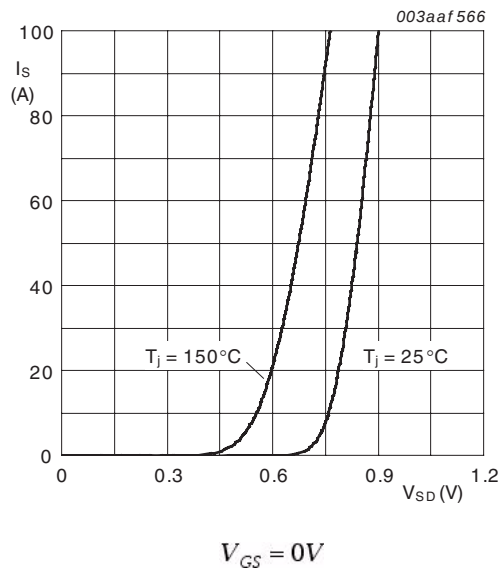


Fig 17. Source current as a function of drain-source voltage; typical values

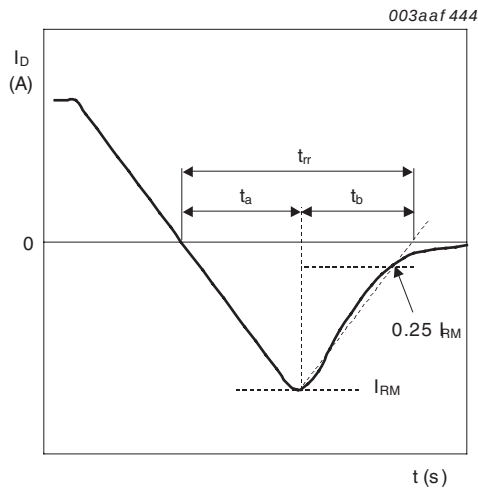


Fig 18. Reverse recovery timing definition

8. Package outline

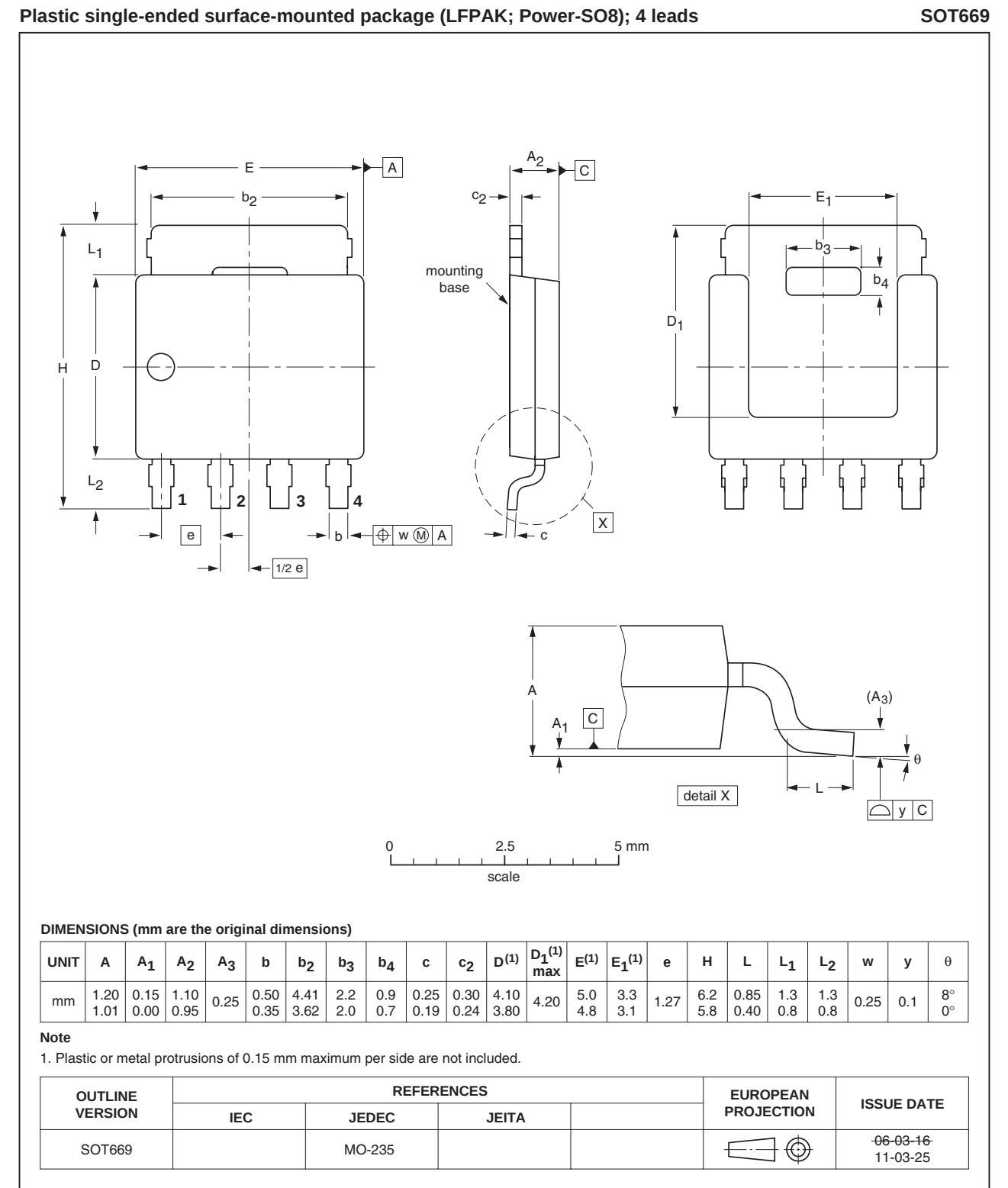


Fig 19. Package outline SOT669 (LPAK; Power-SO8)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R2-30YLC v.1	20110503	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	3
6	Thermal characteristics	5
7	Characteristics	6
8	Package outline	11
9	Revision history	12
10	Legal information	13
10.1	Data sheet status	13
10.2	Definitions	13
10.3	Disclaimers	13
10.4	Trademarks	14
11	Contact information	14

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