

NL MKB Participatiemij
NMP-obligati**Elliott Sound Products****Project 106**

h_{FE} Tester for NPN Power Transistors

© August 2004, Geoff Moss
(with additional material from Rod Elliott)

Introduction

The design objective was to produce an h_{FE} tester with switched collector currents for the DUT (Device Under Test) covering a range suitable for the selection and matching of output transistors for amplifiers such as the JLH Class-A, ESP DoZ etc.

The tester should provide a range of collector test currents from 0.05A to 3A in (roughly) logarithmic steps.

It is important to avoid the need for high power resistors and (rotary) switches with high current rated contacts, especially since the latter can be very difficult to obtain. It is also important to minimise the cost.

Although the circuit may appear complex, it isn't really, but it does test devices at a specified (and fixed) collector current - this is the way that it should be done, but most circuits don't. It is far simpler to fix the base current and measure collector current, but matching devices based on collector current becomes virtually impossible with the fixed base current method.

You may wish to look at Project 177, which uses the same test method, but is far more flexible than the version. It can test both NPN and PNP transistors by simply switching the supply polarity, and is far simpler to build.

Description

Refer to Figure 1 (below). D1 (or U2 shown in Figure 2), R3 and VR1 create an adjustable voltage reference. Rc1-Rc7 resistor values have been selected so that the design collector current flows in the DUT when the voltage across the resistor bank is around 1V. Q1 monitors the voltage across the resistor bank, compares it with the preset voltage reference derived from the LED, and drives sufficient current into the base of the DUT to maintain 1V across the current setting resistors.

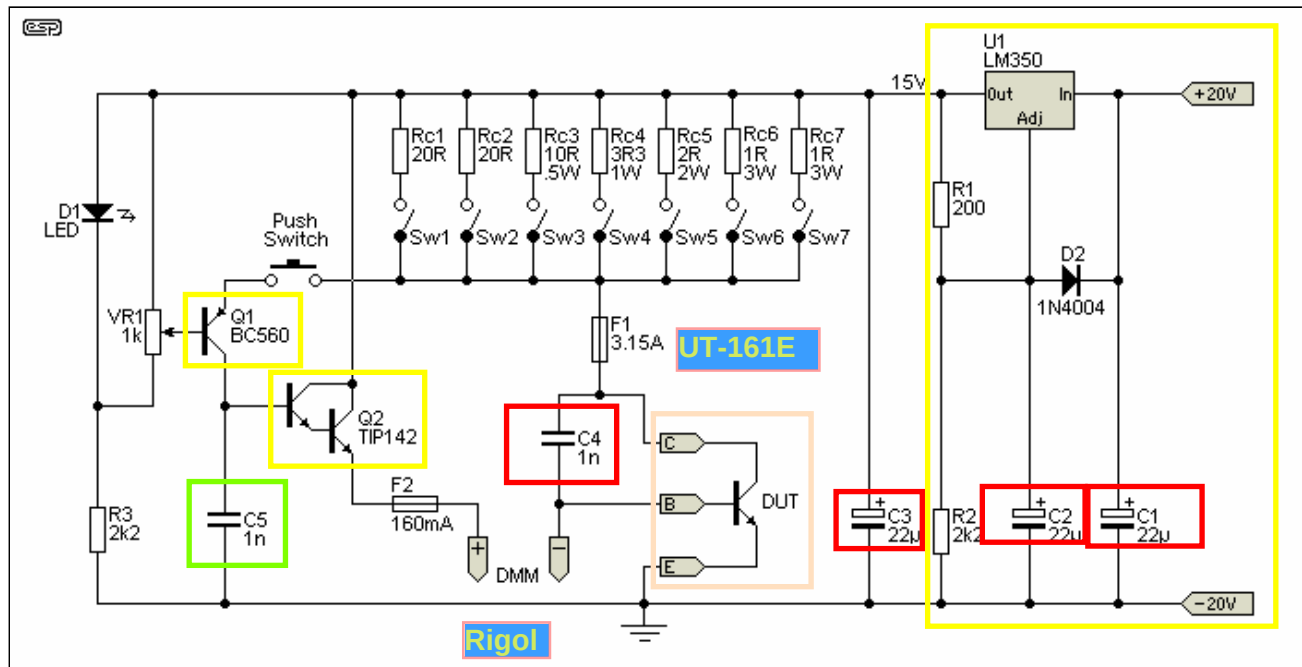


Figure 1 - Circuit Diagram of h_{FE} Tester

Note that the supply is 20V DC. The connection points shown indicate positive and negative, and do *not* mean or imply a dual supply - only the polarity of the connections. Unmarked resistors are 0.25W. Q2, a power Darlington, has been included as a buffer to minimise voltage (and therefore current) variations when DUTs with a low h_{FE} are being tested. SW1 to SW7 should be rated at a minimum of 2A DC.

Fuse F1 provides protection from high collector currents and has been fitted where shown, rather than in the supply rail, so that a 3.15A fuse can be used. If fitted in the supply rail, the next higher standard value (4A) would be needed, thus providing reduced protection. This is because the base current would also be passing through the fuse if it were in the supply rail.

Fuse F2 has been provided to prevent excess base current in the event of the DUT being faulty or incorrectly connected. A resistor in the collector of Q2 could achieve a similar effect but, if large enough to provide sufficient current limiting, the DUT collector current variation for low gain transistors would be outside the design objective of keeping the current constant (for different DUT h_{FE}) to within 1%. A lower value collector resistor for Q2, such that the DUT collector current remained constant, would not limit the DUT base current to below 0.5A and would need to be rated at 10W to prevent failure under fault conditions.

C4 has been included to minimise the possibility of oscillation in the DUT. Because it has been found by a constructor that C4 was not effective, C5 has been added. This makes the circuit unconditionally stable, and oscillation (which will give very odd readings) is not possible with C5 installed. C4 may be left out if you so desire - it is largely redundant with the addition of the extra cap.

rigol 250 mA / 10A

The DMM has been used on its current range, rather than the safer alternative of using it on a voltage range and measuring across a series resistor, because the highest value of series resistor (10R) that could be used in the DUT base circuit, without affecting the accuracy of the DUT collector current, is such that some DMMs will not have sufficient sensitivity to accurately measure the small (mV) voltage generated across the series resistor at the lower DUT collector current settings, particularly if the DUT has a high gain. Note that the reading on the meter is the reverse of DUT current gain - a high reading means a low gain transistor, while a low reading means a high gain device. This is not a limitation, merely something the user should bear in mind.

Those fortunate enough to have a DMM that will accurately resolve a reading to within 0.1mV could, if they so desired, use a 10 Ω (1% or better) resistor in place of the DMM connection shown on the schematic, with meter connection points provided on each side. This allows the meter to be used in voltage measurement mode, with the voltage directly proportional to base current.

Switch Settings and Circuit Notes

The switches SW1-SW7 are used to select the collector current for the DUT. The base current drawn will always be a direct function of the DUT's h_{FE} .

SW1	Off	On	On	On	On	On	On	On
SW2	Off	Off	On	On	On	On	On	On
SW3	Off	Off	Off	On	On	On	On	On
SW4	Off	Off	Off	Off	On	On	On	On
SW5	Off	Off	Off	Off	Off	On	On	On
SW6	Off	Off	Off	Off	Off	Off	On	On
SW7	Off	Off	Off	Off	Off	Off	Off	On
I_C	0A	50mA	100mA	200mA	500mA	1A	2A	3A

Table 1 - Switch Settings Vs. Collector Current

With the sequential switching shown on the schematic, the DUT collector currents are as shown in Table 1. The 3A range can be left out, if desired by omitting SW7 and Rc7. The 0.05A range can be left out by omitting SW1 and Rc1 and changing Rc2 to 10R (0.5W).

If the 3A range is left out, the voltage regulator can probably be an LM317K since the typical current limit for this device is 2.2A, but constructors should note that the LM317K is only guaranteed up to 1.5A so current limiting could be experienced on the 2A range.

An LM338K could be used in place of the LM350K but then fuse F1 is (even more) essential since the current limiting of an LM338K doesn't kick in until something over 9A compared to 4.5A for the LM350K. With any of the IC regulator options shown, you will need a good heatsink. Power dissipation in the regulator is determined by the voltage across the IC, and current through it. Worst case current will be a little over 3A (including base current), and approximately 5-7V across the regulator IC itself. This represents a dissipation of up to about 22W or so. Choose a relatively large heatsink, and watch your mounting techniques carefully to ensure best thermal transfer. A fan may be used if desired, and is recommended if regular use at high current is anticipated. For normal intermittent duty, a 1°C/W heatsink will probably be quite adequate.

The suggested supply voltage is 15V (to suit alternative fixed voltage regulators and cheap, surplus power supply units). This gives a test voltage that is reasonably close to the expected V_{ce} in the final amplifier circuit whilst keeping the DUT power dissipation at a reasonable level.

The supply voltage could be increased to say 21V (to give a test V_{ce} of 20V) but the 3A range would need to be dispensed with (IMO). Conversely, the supply voltage could be reduced to 6V (V_{ce} 5V) so that higher test currents could be used or to permit comparison of measured results with data sheet figures. If the supply voltage is reduced, the value of R3 will need to be reduced as well to maintain a suitable current through the voltage reference and VR1. You will need to make your own calculations for regulator dissipation.

Q1 is not critical and can be any small signal PNP transistor with a specification comparable to that of a BC560. Q2 is also not critical and can be any NPN power Darlington with a similar specification to that of a TIP142. Note that a heatsink is

highly recommended for Q2, given that dissipation may be as high as 4.5W at maximum base current for a very low gain device (typically 300mA, although this will blow the 160mA fuse) - see below for more information.

Fuses F1 and F2 should be quick blow (and plenty of spares should be kept handy 😊).

The push switch has been positioned between the resistor bank and Q1 so that when measurements are not being taken, there is no current flow through Q1. If the push switch were located in the more usual position (in series with F2 and the DMM), whenever the push switch was open (most of the time) there would be a 4mA+ current through Q1.

Initial Setup

A spare, expendable DUT (on a suitable heatsink) is connected and a link inserted in place of the DMM. With the push switch and SW7 (only) - SW6 if the 3A range is omitted - made, VR1 is adjusted to give 1V across Rc7 (or Rc6).

A DMM (on an appropriate current range) is inserted in the collector lead of the DUT and the collector current measured at each of the sequential switch positions which set the collector current. These currents are used for future h_{FE} calculations (see below).

All switches are then returned to the open position, the DUT and DMM link are removed and the tester is ready for use.

Using the Tester

The DUT is connected (mounted on a suitable heatsink), along with the DMM (initially set to the 200mA current range). SW1 is closed and the push switch operated. A DMM reading is taken when the display has stabilised (the DMM current range may need to be lowered for this switch position). The push switch is released, SW2 is closed, the push switch is remade and another reading is taken. Repeat until all toggle switches are closed, then reset all of the toggle switches to open. Every attempt should be made to keep the speed at which the toggle switches are actuated constant between tests on different DUTs, so that the temperature rise in the DUTs is approximately the same. This is because h_{FE} varies according to the transistor junction temperature.

Alternatively, the push switch can be held closed whilst the toggle switches are sequentially actuated, with readings being taken after each switch operation. If anything untoward is observed (or smelt) during the test, release the push switch immediately.

The h_{FE} at each of the collector currents can be calculated from the collector currents measured during the initial setting up and the base currents measured during the test sequence (a spreadsheet comes in handy here). The preset collector currents may not be exactly spot on due to resistor tolerances (+/-5%) but they will remain virtually unchanged (within about 1%) for DUT gain variations between 25 and 200.

To calculate the h_{FE} for any collector current (I_c), use the simple formula ...

$$h_{FE} = I_c / I_b \text{ (where } I_b \text{ is base current)}$$

For example, if the collector were measured at 3A, and base current measured at 83mA, h_{FE} is ...

$$h_{FE} = 3 / 0.083 = 36$$

When disconnecting the DMM after completion of measurements remember to move the leads back to the voltage measuring position.

Appendix

This section includes some additional notes that you may find useful ...

Some more information about heatsinking Q2 ... The maximum (no fault) dissipation in Q2 (DUT gain 25, DUT I_c 3A) is just over 1.5W. With a junction-air thermal resistance of 35°C/W, and (very) intermittent operation at maximum dissipation levels, no heatsinking should be necessary. However, it would be prudent, particularly in a totally enclosed case, to mount the TIP142 onto a metal chassis if available. Otherwise, fit a small heatsink (say around 10°C/W, or even a small sheet of aluminium).

As regards the heatsink for the DUT, the maximum dissipation is 45W with the proposed rail voltage and maximum I_c , though this is intermittent and of short duration. Allowing for a maximum junction-case thermal resistance of 1.5°C/W and an isolated heatsink (so no mica or SilPad - thermal grease is highly recommended though), under continuous 45W dissipation a heatsink rated at better than 0.4°C/W would be necessary to keep the junction temperature below 130°C. Obviously, the intermittent nature and short duration of the maximum dissipation means that something smaller can be used. I was thinking of something between 1 and 2°C/W, which would allow for an average dissipation over the course of the tests of around 20W, even with devices having a relatively poor j-c thermal performance.

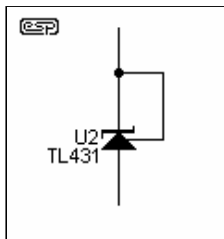


Figure 2

As mentioned above, an alternative to the LED is a TL431 voltage reference IC. The connection scheme is shown to the left, and the IC is wired in place of the LED. No other changes to the circuit are needed. While this is undoubtedly more accurate than the LED, the improvement in real terms will probably not be worth the effort.

In Geoff's original circuits, the 3 electrolytic capacitors were specified as either 1µF tantalum or 22µF aluminium electros. Regular readers will be aware of my hatred of tantalum caps (the most unreliable capacitor ever made), so I only recommend the aluminium electrolytic option.

It is also likely that you will need a suitable power supply. This should be fairly robust, but make sure that the loaded voltage is reasonably close to 20V (assuming the 15V supply recommended). If the input voltage is too high, the regulator's dissipation will increase, placing greater demands on the heatsink.

The supply will typically use a dual 15V toroidal transformer, with the windings in parallel for maximum current. Unloaded voltage will be in the order of 25V, dropping to around 20V at full load. The transformer should be rated for around 80-100VA, but a 160VA (typical of toroidal transformers) will do very nicely. A 25A bridge rectifier and a minimum of 4,700µF should be used for rectification and filtering respectively. More capacitance can be used if you want, but will not improve the performance. Figure 3 shows a typical supply.

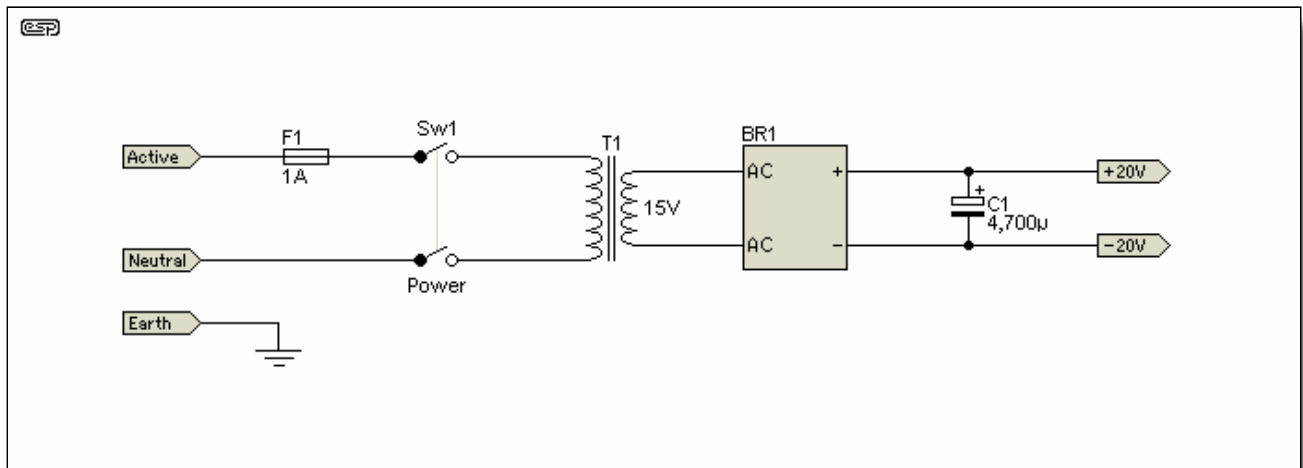


Figure 3 - Power Supply

There is nothing special about the supply, but the usual precautions must be taken to ensure that no-one can make accidental contact with any mains wiring. Naturally, a 'conventional' E-I transformer may also be used if one is to hand or can be obtained for the right price. **A secondary current rating of at least 5A is recommended to prevent the voltage from collapsing too much** when the load is applied.

As noted, this tester is designed for **NPN power transistors**, and it is obvious that it will be difficult to make the unit dual polarity so that PNP devices can be tested as well. Essentially, there are **several ways to make the tester able to test both NPN and PNP devices**, but it is not an especially trivial exercise. It **may be easier to duplicate the entire tester section**, using a **reversed LED**, and **with an NPN transistor instead of PNP and vice versa**. The polarity of the DC at the regulator output needs to be reversed, and it would probably be easiest to use relays to switch the polarity and base current driver circuits. This is especially true because of the number of connections that must be changed. Only the base drive circuit needs to be duplicated for the opposite polarity - the remainder of the circuit is passive and not polarity sensitive.

Note that getting a **high current version of any regulator** is no longer easy. TO3 types sell for astonishing prices, and it will almost certainly be necessary to use some other arrangement to obtain the current needed. Probably the easiest is to **use 7815 fixed regulators in parallel**, with a **current balancing resistor at the output** of each. These should **not be less than ~0.22 ohms 1W**, and I'd recommend that **three 7812 regulators be used**, with a **maximum current of 1A each**. This distributes the heat better (each will dissipate about 5W), which is important given the **rather poor heat dissipation capabilities of the TO220 package**. This arrangement will work very well, and it will be easy to keep the regulators at a sensible temperature. A heatsink is mandatory of course, but it need not be particularly large. 1°C/ watt allows a 15°C temperature rise for the regulators at 1A each. For intermittent operation, the heatsink can be smaller.

It will be left as an **exercise for the constructor to figure out the PNP version, based on the description above**.



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