OX 8620 / OX 8627
DIGITAL/ANALOG
OSCILLOSCOPE

Maintenance Manual

metrix

IM1166G - Ed. 1 - 11/97

CONTENTS

CHAPTER 3 - ANALOG BOARD ADJUSTMENT .....33 to 47

CHAPTER 4 - DIGITAL BOARD DESCRIPTION

CHAPTER 5 - DIGITAL BOARD ADJUSTMENT

ANNEXES

ANNEX 1 : GENERAL SYNOPTIC
FRONT PANEL SYNOPTIC

ANNEX 2 : SCHEMATICS - CI 2086-05.1 + COMPONENTS LOCATION
SCHEMATICS - CI 2086-08 + COMPONENTS LOCATION

ANNEX 3 : DIGITAL BOARD SCHEMATICS
OX 8620 ---> HD 1935
OX 8627 ---> HD 1936
---> HD 1887

ANNEX 4 : MODIFICATIONS

ANNEX 5 : PARTS LIST

CHAPTER 1 - SPECIFICATIONS

Only the values assigned tolerances or limits are guaranteed values. Values without tolerances are given for information only, without guarantee.

1. VERTICAL DEFLECTION

CH1 - CH2	Specifications	Comments
Bandwidth -3 dB in BWL	> 100 MHz ≈ 20 MHz	
Rise time	< 3.5 ns	
Vertical deflection factor (sensitivity)	Ranges: 2 mV/div to 5 V/div ± 3%	11 positions 1-2-5 sequences
Variable vertical deflection factors	Multiplication of V/div range by 1 to 2.5 (reducing displayed signal amplitude)	Calibrated position: control in left end stop position, LED off. Uncalibrated position: LED on.
Max. input voltage	Protection : ± 400 V CAT II (DC + peak AC to 1 kHz)	
Level limitation / frequency	DC to 3 MHz 400 Vrms from 3MHz to 100MHz : - 20dB/decade	
Focused trace thickness	< 2 mm	
Chopping frequency (CHOP)	500 kHz approx.	
Input coupling	DC: 0 to 100 MHz AC: 10 Hz to 100 MHz GND: 0 V reference	
Input impedance	1 Mohm ± 1% // 15 pF	
Squarewave signal response	Overshoot < 5% Aberration at 10 mV/div - on plateau < 1 mm - on edge < 2 mm	 1 kHz to 1 MHz 1 MHz (Rise time < 100 ps)
Crosstalk	42 dB typ. (2 mV/div : 36 dB typ)	until 100 MHz, same sensitivity on CH1 and CH2, 6div.
Display	CH1 : CH1 only CH2 : CH2 only ALT : CH1 then CH2 alternating CHOP : CH1 and CH2 chopped ADD : CH1 + CH2 or CH1 - CH2 XY : X = CH1 and Y = CH2	

2. HORIZONTAL DEFLECTION (TIMEBASE)

A - B	Specifications	Comments
Sweep speed	Ranges 50 ns to 100 ms/div ± 3%	20 positions 1-2-5 sequences
Variable factor (A only)	Modification of ms/div range by 1 to 2.5 (signal horizontally contracted)	Calibrated position: control in left end stop position, led off.
		Uncalibrated position: led on.
x 10 expansion	Accuracy: ± 5%	Gives 5 ns/div
HOLDOFF	1 to 10, variable	
XY mode	X = CH1: DC coupling: 0 Hz to 4 MHz AC coupling: 10 Hz to 4 MHz Y = CH2: DC coupling : 0 Hz to 100 MHz AC coupling 10 Hz to 100 Mhz Phase difference < 1.5° at 100 kHz	

3. TRIGGER SYSTEM

	Specifications		Comments
Sources	*Sensitivity in normal mode: Triggering from 0 to 180 MHz.*		
CH1	0.5 div	to 1 kHz	
or	1 div	to 100 MHz	
CH2	2 div	to160 MHz	
ALT			Source according to display mode: CH1 trigger CH1 ALT trigger CH1 then CH2 CHOP trigger CH1 ADD trigger CH1 CH2 trigger CH2 -CH2 trigger CH2
LINE	-		
EXT	100 mVrms	0 to 50 MHz	protection ± 400 V (DC + AC peak, f < 1 kHz) CAT II
	200 mVrms	50 to 100 MHz	
Filters	*Bandwidth:*		
	AC	10 Hz to 180 MHz	
	DC	0 Hz to 180 MHz	
	LFR (rejection)	10 kHz to 180 MHz	
	HFR (rejection)	0 Hz to 10 kHz	
	TVH : synchronize video signal on line pulses		
	TVV : synchronize video signal on field pulses		
Horizontal mode	AUTO		Relaxed mode
	Normal		Triggered mode
Slope	Negative-going edge		
	Positive-going edge		
Level	*Adjustment range:*		
	P-P: between signal minimum and maximum		
	Normal: ± 12 divisions		

3. DIGITAL MEMORY

Acquisition

- One converter per channel
- Vertical resolution: 8 bits (256 levels).
- Accuracy: 3% for the complete system.
- Sampling frequency: 40 MHz.
- Memory capacity:
  - . OX 8620: two 4 K buffers,
  - . OX 8627: four 8 K buffers.

  Saving and comparing recorded signals.
- Acquisition modes:
  - . ROLL: 200 ms to 200 s/div (continuous scrolling or triggered stop).
  - . REFRESH: 0.1 µs to 200 s/div
  - . SINGLE: 0.1 µs to 200 s/div (single shot).

☞ ***Notes:***
- . ***Envelope mode available with REFRESH (repeated signals).***
- . ***Glitch mode (OX 8627): Capture of events > 50 ns from 200 ms to 10 µs/div.***

- Pretrigger.

  In 1 K steps.
  - . OX 8620: 0, 1, 2, 3, 4 K
  - . OX 8627: 0, 1, 2, 3, 4, 5, 6, 7, 8, K

Display

- Readout: in analogue and digital mode (switchable).
- Channel selection: according to vertical mode.

- Signal analysis:

  . Vertical offset (during and after acquisition),
  . Horizontal offset,
  . Expansion, movement (bar graph),
  . Linear and sinusoidal interpolation.

Measurements

Measurements are available in analogue and digital mode.

- By cursor: Voltage, time, frequency and phase.
  Reference selection (CH1 or CH2).

- Automatic: 17 automatic measurements are available

Vpp	peak-to-peak voltage	F	frequency
Vavg	average voltage	tr	rise time (10% to 90%)
T	period	W+	positive pulse width > 0 (at 50%)
tf	fall time (90% to 10%)	DC+	W+/T duty cycle
W-	negative pulse width < 0 (at 50%)	Vma x	maximum voltage
DC-	W-/T duty cycle	Vmin	minimum voltage
Vh	high voltage	Vlow	low voltage
Vamp	amplitude	φ	phase
Vrms	root mean square voltage		

☞ ***Note:*** ***Automatic measurements are taken on stored signals; this part must include at least one and a half periods (four edges) except for Vrms and Vavg (if less than a period and a half, the calculation is performed on the 1000 points on the screen).***

4. MEASUREMENTS RELATIVE PRECISION

1. Amplitude measurement

* P = 3% + 8 / Amplitude (div.) For 8 div : P = 4%

* Frequency comportment (sinus signal)
  You must have at least 20 samples for each signal period of frequency max 1 MHz. The results are significant up to a frequency of 7 MHz.

2. Time measurement

2.1	t/div ≥ 5 µs/div	P = 0,01% + 2 * [t/div (µs)] / [Tmesured (µs)]
2.2	t/div < 5 µs/div	P = 0,01% + 5 / [Tmesured (µs)]

3. Frequency measurement

3.1	t/div ≥ 5 µs/div	P = 0,01% + 2 * [t/div (µs)] * [Fmesured (MHz)]
3.2	t/div < 5 µs/div	P = 0,01% + 5 * [Fmesured (MHz)]

Hard copy

Supports

Devices

HPGL	HPGL devices (Ex : TX7130, TX7131)
IBM Pr	Quadruple density dot matrix printers (Ex : IBM Proprinter XL24)
ESC P2	Epson ink jet printers (Ex : Stylus 800+)
HP-PCL	Laser printers (Ex : HP Laser Jet IIP)

Interfaces

RS 232	Serial port
IEEE	IEEE Bus(OX 8627)
Centro	Centronics (HA 1251 accessory)

Options

- print graticule,
- print configuration,
- print text,
- print quarter page partitions (HPGL digital plotters only).

Communication interfaces

Uses Hard copy or remote programming (SCPI language).

RS232

- baud rate: 50, 75, 110, 150, 300, 600, 1200, 2400, 4800, 9600
- parity: none, even, odd
- data bits: 7 or 8
- stop bits: 1 or 2
- protocol: Xon/Xoff or RTS

IEEE (OX 8627 only)

- address: 0 to 30

5. MISCELLANEOUS

Calibration signal

Shape	squarewave
Amplitude	-0.5 V ± 1% CAT I
Frequency	10 kHz to 50 kHz

Z modulation

Input	BNC socket on rear panel
Sensitivity	TTL level
Input resistance	10 kΩ
Bandwidth	20 MHz
Maximum voltage	± 50 VDC CAT I

6. GENERAL FEATURES

CRT

Type	rectangular with internal graticule, 13 cm diagonal
Graticule	8 vertical divisions with five sub-divisions 10 horizontal divisions with five sub-divisions 1 division = 1 cm
Screen	average persistence phosphor GY
Trace	trace rotate adjustment focus adjustment intensity adjustment
Total acceleration voltage	15.5 kV.

Contrast screen.

Power supply

Mains: automatic selection, 94 to 264 Vrms, 45 Hz to 440 Hz. CAT I I
Removable mains power cord.
Cord winder with plug support on back of instrument.
Consumption: < 70 W

Safety

According IEC 1010-1 (NF C 42-020 (1993)):

- insulation: class 1,
- degree of pollution: 2,
- input overvoltage category: CAT II (400 V),
- power supply overvoltage category: CAT II (264 V).

Environment

Use	inside	
Altitude	< 2000 m	
Reference temperature	+18°C	to +28°C
Range of use	+10°C	to +40°C
Operating temperature	0°C	to +40°C
Storage range	-20°C	to +70°C
Relative humidity	< 80% RH	up to +31°C

Electromagnetic compatibility CE

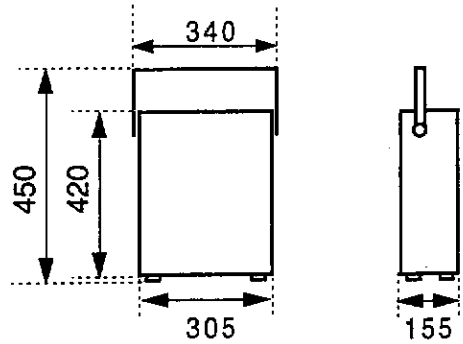
Susceptibility and pertubations complies with NF EN 550011, VDE 871, IEC 801 standards.

Mechanical features

Stackable, with handle which also doubles as stand.

Dimensions : See figure below.

Weight: ≈ 6 kg



Packaging

Dimensions: 580 x 500 x 380.

Weight: ≈ 7 kg

CHAPTER 2 - ANALOG MOTHER BOARD

Content

Global Over-view : See sheet GENERAL SYNOPTIC - cf. Annex 1

This sheet is very usefull to adress quickly the right sheets of schematic you need. For example you've got a problem on CH1 attenuator then refer to sheet 3/19 - cf. Annex 2. First of all you must look at the printer circuit board reference - cf. Annex 1.

Functional Analysis	Schematic situation
- POWER SUPPLY	sheet 1/19 & sheet 2/19
- InputsY1,Y2	sheet 3/19 & sheet 4/19
- Channel mixing and synchro	sheet 5/19, 6/19, 7/19
- Trigger	sheet 7/19
- Y amplifier	sheet 8/19, 9/19, 13/19
- A & B time base	sheet 10/19 & sheet 11/19
- Vertical, Horizontal and Lighting logic	sheet 12/19
- Lighting amplifier	sheet 2/19 & 13/19
- X amplifier	sheet 14/19
- µP Interface	sheet 15/19
- Digital to Analog converters	sheet 15/19 & 16/19
- Front Pannel	sheet 17/19, 18/19, 19/19

symbols

VCC12 : positive voltage of 12v
VEE5 : negative voltage of 5v
VAA110 : 110v before rectifying
Numbers in circles near connectors refers to corresponding sheets
Values in brackets unders components refer to OX8620/OX8627 components values
NC : means not connected

1. POWER SUPPLY

1.1 LOW VOLTAGES - Sheet 1/10

It is a flyback SMPS regulated from the 5V output via R114/R113 voltage divider, Z104 reference integrator, Z105 OPTO coupler, and Z101 current mode SMPS controler. Intensity is sensed into R131...R133.
First of all, Power cord is connected on J104, neutral pass trought R101: CTN10 INRUSH current limiting, and line via F101. Switch S101 is the ON/OFF main switch. Line filter consits of C100, L101, C102.
AC is rectified by D101 and C104. R117,104,105..Z102,Z103 are used to delivering 50Hz signal and LINE SYNC.
50Hz signal is involved in the power down process in order to back-up the front pannel settings.
LINE SYNC is used in the trigger.
Voltage divider R146 to R135 is the starter supply
Q103,Q104 are used in the protection against output shorts and rectifiers failures.
Protection acts if necessary since power on and until power down with a recovery delay of about 5 seconds.

SMPTS DIAGNOSTICS and REPAIRS

WARNING RISK OF ELECTRIC SCHOCKS
Be carrefull of high voltages and uses isolation transformer before connecting a grounded scope on power supply. C104 should be discharged before any sort of repairs on the primary side SMPS.

In case of Primary side **flash** you should replace :
Q101, R131, R132, R133, R120, R118, R119, D113, D105, Q103, Q104, Z101 and all other extra components which seems failed.

In case of systematic shut down just a few seconds after start, you should verify secondery rectifiers and outputs. The right method consists in removing one rectifier and then tries to start again without it. If start is OK you have found the output or the rectifier which is damaged.

1.2 HT AND THT

WARNING RISK OF ELECTRIC SHOCKS

Disconnect the line cord. Discharge the CRT anode. Don't short circuit but use a THT resistor or a THT probe connected to ground to do it. If not, risk of electric damages in the bright circuitery.

These two voltages respectively -2275v and +13500v are supplied by the module M201 and a few external components. M201 contains a voltage multiplyer by six for the THT output, the -2275V rectifier and a resonnant transformer which form in addition with Q211 an HARTLEY oscillator. Output voltage is sinusoidal and amplitude is regulated by Z201 which compares C234 potential with VCC12 (R242,243,R241)/(R225+R231...R236).Voltage on pin 7 of Z201 indicate the power rate of this supply. No THT and +13v on pin7 indicate: short circuit or M201 failure a normal value is negative .

1.3 FOC

This voltage is adjustable with COM_FOC front panel potentiometer. Q210 and D235 acts as an amplitude modulator on the signal VAA110. The result is transmitted via C227 to D234 which rectifies the result across C232//R253. Q205 is involved in focus-track system.

2. **INPUTS Y1 & Y2** **Sheets 3/19 & 4/19 parts references are for CH1 - See** Annex 2

These two channels consist in 1MΩ frequency compensated attenuators, High impedance HF amplifier, and 50 Ohms output attenuator. HF high impedance amplifier bias is controlled by a regulation loop R334/R375+R346, R338, R345, R310 Z301, R330, R331, Q303, R333.
OP-AMP Z301 consists in an integrator which compares input and output bias of HF amplifier and then, sets the right curent in Q303 to minimise the difference. R346 should be adjusted to obtain an undistored 1kHz square wave response
High impedance attenuator consists in two cells 1/10 and 1/20. The two relays in combination allow: 1/1 1/10 1/20 1/200 attenuation ratios.
Low impedance attenuator consists in a voltage divider with 1/1 1/2 1/4 1/5 and GND taps. Switching transistors Q308 to Q312 connect the right taps to "ATT_CH1" output
Q318, Q319, D304 are the protection against overload voltages and transients.
All the channel is configured with TTL commands :HI1_10, HI1_20,DC_AC1
BI1_1, BI1_2, BI1_4, BI1_5, BI1_GND

PROGRAMMATION TABLE

SENSIVITY CHANNEL Y1

VOLT/DIV	HI1_20	HI1_10	BI1_5	BI1_4	BI1_2	BI1_1	GY1X2_5	BI1_GND
0div/mv	T	T	F	F	F	F	CFG	T
5v/div	T	T	T	F	F	F	F	F
2v/div	T	T	F	F	T	F	F	F
1v/div	T	T	F	F	F	T	F	F
.5v/div	T	F	T	F	F	F	F	F
.2v/div	T	F	F	F	T	F	F	F
.1v/div	F	T	F	F	T	F	F	F
50mv/div	F	T	F	F	F	T	F	F
20mv/div	F	F	F	T	F	F	F	F
10mv/div	F	F	F	F	T	F	F	F
5mv/div	F	F	F	F	F	T	F	F
2mv/div	F	F	F	F	F	T	T	F

COUPLING	DC_AC1	BI1_GND
DC	T	F
AC	F	F
GND	T	T

SENSIVITY CHANNEL Y2

VOLT/DIV	HI2_20	HI2_10	BI2_5	BI2_4	BI2_2	BI2_1	GY2X2_5	BI2_GND
0div/mv	T	T	F	F	F	F	CFG	T
5v/div	T	T	T	F	F	F	F	F
2v/div	T	T	F	F	T	F	F	F
1v/div	T	T	F	F	F	T	F	F
.5v/div	T	F	T	F	F	F	F	F
.2v/div	T	F	F	F	T	F	F	F
.1v/div	F	T	F	F	T	F	F	F
50mv/div	F	T	F	F	F	T	F	F
20mv/div	F	F	F	T	F	F	F	F
10mv/div	F	F	F	F	T	F	F	F
5mv/div	F	F	F	F	F	T	F	F
2mv/div	F	F	F	F	F	T	T	F

COUPLING	DC_AC2	BI2_GND
DC	T	F
AC	F	F
GND	T	T

3. MUX CH1 & MUX CH2 - Sheets 5/19 & 6/19 - See Annex 2

Parts reference are for Mux CH1

These two circuits use a Métrix ASIC's Z501. Internal functions are: Variable Gain, Position, Channel Inversion, Channel selection, Synchro selection, Synchro inversion, Memory analog interface.

3.1 LIST OF SIGNALS - Sheet 5/19 - See Annex 2

VOS_MUX1 : Input Off-set control of Z501 (DAC_8 from fig 16/19)
ATT_CH1 : Analog CH1 INPUT (from fig 4/19)
VAL_CAD_CH1 : Digital control of position and outputs B+,B-,C+,C- (true normal, false X/Y)
GY1X2_5 : Digital command of CH1 gain (true = gain x 2.5)
VALID_CH1 : Digital command of CH1 (true enable CH1)
SGN_VIDEO : Digital command choice between video and video negative
VAL_PRE_SY1 : Digital command choice of trigger source
CAD_CH1 : Analog signal Position CH1
VAR_ADJ1 : Analog signal Gain control of CH1
VAR_CH1 : Analog signal GVAR front pannel control
SIGNAL_X : Analog output of CH1 in X/Y mode
CENT_XY : Output Off-set control of Z501 in X/Y mode
PRE_NUM1_1 : differential output for analog memory interface not use in PRE_NUM1_2 : OX 8620
INTER_1_CH1 : Differential current bus for main Y signal
INTER_2_CH1 : idem
PRE_SYNC1 : Differential current bus for Sync signal
PRE_SYNC2 : idem

3.2 LIST OF SIGNALS - Sheet 6/19 - See Annex 2

VOS_MUX2 : Input Off-set control of Z601 (DAC_8 from fig 16/19)
ATT_CH2 : Analog CH2 INPUT (from fig 4/19)
VAL_CAD_CH2 : Enable position control of CH2
GY1X2_5 : Digital command of CH2 gain (true = gain x 2.5)
VALID_CH2 : Digital command of CH2 (true enable CH1)
SGN_VIDEO : Digital command choice between video and video negative
VAL_PRE_SY2 : Digital command choice of trigger source
CAD_CH2 : Analog signal Position CH2
VAR_ADJ2 : Analog control of gain CH2 (DAC_8 from fig 16/19)
VOS_DEC2 : output off_set control of Z601
VAR_CH2 : Analog signal GVAR front pannel control
PRE_NUM2_1 : Differential output for analog memory interface not use in PRE_NUM2_2 : OX 8620
INTER_1_CH2 : Differential current bus for main Y signal
INTER_2_CH2 : idem
PRE_SYNC1 : Differential current bus for Sync signal
PRE_SYNC2: idem
VOS_SYNC1 : Trigger off_set control of CH1 (DAC_4 from sheet 15/19)
VOS_SYNC2_EXT : Trigger off_set control of CH2 & EXT (DAC_4)
SYNC_ANA : Analog mixed output for triggering operation

3.3 PROGRAMMATION TABLE

MODES Y	/VISU_CH1	/VISU_CH2	CHOP	CAL Y1	CAL Y2	XY	VAL_CAD_CH1
CH1	T	F	F	CFG	0div/mv	F	T
CH2	F	T	F	0div/mv	CFG	F	T
CH1 alt CH2	T	T	F	CFG	CFG	F	T
CH1 chp CH2	T	T	T	CFG	CFG	F	T
CH1 + CH2	F	F	F	CFG	CFG	F	T
XY	F	F	F	CFG	CFG	T	F

4. TRIGGER - Sheet 7/19 - See Annex 2

4.1 EXT INPUT

First of all this signal is attenuated then passes via a HF buffer which drives Z704 analog input. Z704 only amplifies and mixes the different trigger sources on the common differential trigger BUS (PRE_SYN1, PRE_SYNC2).

C_SYN_EXT : Digital command: ENABLE the external triggering mode
SGN_VIDEO : Digital command:choice between video and video negative

4.2 VIDEO SEPARATOR

Q703,Q704,Q705,Z702 and some analog glue are used to separate vertical sync and composit sync.

_TVE : Digital command: actif low ENABLE TV modes
TVV_TVH : Digital command: vertical or horizontal trigger
SYNC_ANA : Analog signal for triggering

4.3 SYNCHRO FILTERS

Main analog signal SYNC_ANA is divided in two parts. BF spectrum passes through Z701pin3 to 4, Z709 buffer, Z701 pin2 to 15 and R743. HF spectrum passes through Q706, C726 and join the BF way on Z701 pin13. Z701 Pin 14 delivers the filtered signal or line synchro.

4.4 TRIGGER

First of all, analog synchro signal from Z701 pin 14 OR Z702 pin14 passes via a HF buffer and then drive the main ECL trigger Z707 via R784 and, the PTP rectifier via R767. Q710,Q711,Q712 translates the ECL output level of Z707 in a TTL level and acts as a slope selector. Level is transmitted from the front pannel via Z708, R749, R780. The front pannel PCB switch LEVEL signal from three sources. LEVEL front pannel potentiometer, PTP rectifier, DACLEVEL is from a DAC_4 common with the TRACE SEP command. This last source is used in the AUTOSET process.

4.5 PROGRAMMATION TABLES

SOURCE	/PRE_CH1	/PRE_CH2	Y/LINE_E	SYNC_EXT
CH1	F	T	T	F
CH2	T	F	T	F
CH1 alt CH2	T	T	T	F
LINE	F	F	F	F
EXT	F	T	T	T

FILTERS	DC_E	AC_E	HFR	/TVE	TVV/TVH
DC	T	F	F	T	X
AC	T	T	F	T	X
LFR	F	F	F	T	X
HFR	T	F	T	T	X
TVH	F	F	T	F	T
TVV	F	F	T	F	F
OFF	F	F	T	T	X

SLOPE	SLOPE+
normal +	T
normal -	F
TVV +	F
TVV -	F
TVH +	T
TVH -	T
LINE +	F
LINE -	T

VIDEO	SLOPE+	SGN_VIDEO
+	F	T
-	F	F

5. Y AMPLIFIER MIDLE SECTION - sheet 8/19 - See Annex 2

It's a differential chain. Inputs consist in the two currents bus INTER_1, INTER_2. The first stage Q801,Q802 is a common base amplifier which convert current in voltage and then drives Q821, Q819 common collector driver. Then via the bandwidth limit filter, signal drive Q804, Q805, Q808, Q807 cascod amplifier. After that we've just a last buffer Q809, Q810 to drive the delay line.

INUM_Y1,INUM_Y2 is an auxiliary input which is used in restitution mode for the OX8620, OX8627.
Q818, Q822, Q817 is the trace separator system. TRACE SEP amplitude is supplied by a DAC_4 converter.

6. AMPLIFIER DRIVER - sheet 9/19 & 13/19 - See Annex 2

It's a differential chain inputs consist in YDL1, YDL2. First stage Q901, Q902 match the delay line impedance and drive the second cascod stage Q903, Q904 and Q905, Q906. Next stage is just a common collector driver. The last cascode stage is built on Q909...Q914 and Q915, Q916 on sheet 13/19.

Z901 is the bias control of the output stage.

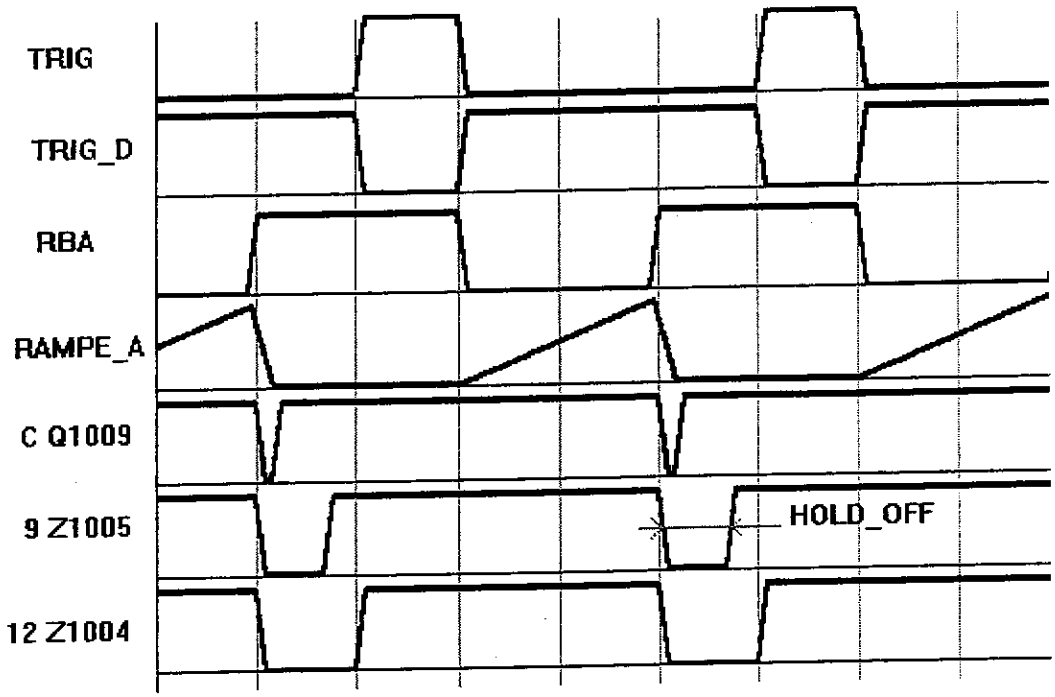
7. TIME BASE A - sheet 10/19 - See Annex 2

7.1 THEORY OF OPERATION

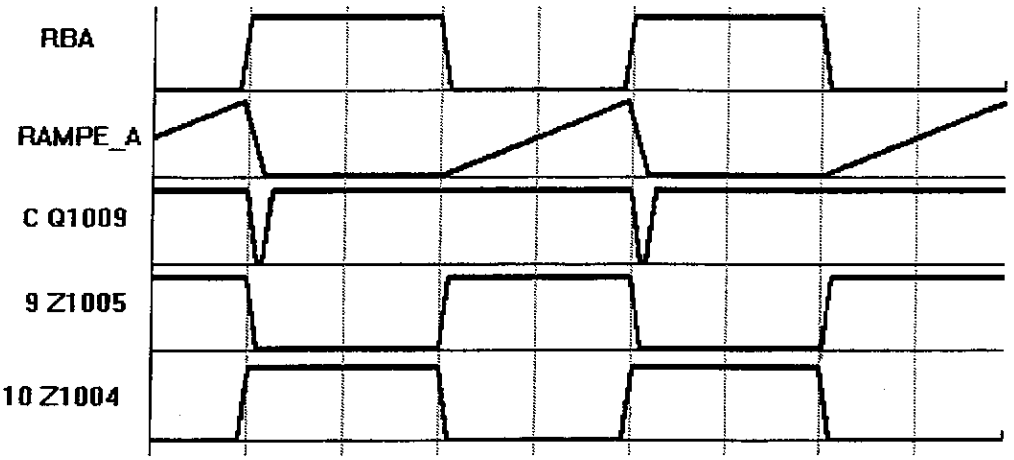
This saw-tooth generator is based on the constant current charge of a capacitor the main parts are :

Capacitance switching	:	K1001, C1003, C1002
Constant current generator	:	Z1003(1.2.3), Q1001, divider R101 to R1055, Z1001, Z1002, Z1006, Q1003, Q1004
High impedance buffer	:	Z1003(5.6.7), Q1006, Q1007, Q1008
End ramp level detector	:	R1028, R10029, R1030, R10034, R1041, Q1009
Hold off timer	:	Z1005(9.10), C1008, C1007, C1023, C1024
Norm/Auto flip flop	:	Z1004 & timer Z1005
TRIGGER flip flop	:	Z1010
Triggered timer	:	Z1005

7.2 WAVEFORMS OF NORM MODE



7.3 WAVEFORMS IN AUTO MODE WITHOUT TRIGGER



7.4 PROGAMMATION TABLE

T/DIV A	VIT LNT A	BOND RA	UA2	UA1	UA0
100ms	T	T	F	F	T
50ms	T	T	F	T	F
20ms	T	T	F	T	T
10ms	T	T	T	F	F
5ms	T	T	T	F	T
2ms	T	F	F	F	F
1ms	T	F	F	F	T
0.5ms	T	F	F	T	F
0.2ms	T	F	F	T	T
100µs	T	F	T	F	F
50µs	T	F	T	F	T
20µs	F	T	F	T	T
10µs	F	T	T	F	F
5µs	F	T	T	F	T
2µs	F	F	F	F	F
1µs	F	F	F	F	T
0.5µs	F	F	F	T	F
0.2µs	F	F	F	T	T
100ns	F	F	T	F	F
50ns	F	F	T	F	T

8. TIME BASE B - sheet 11/19 - See Annex 2

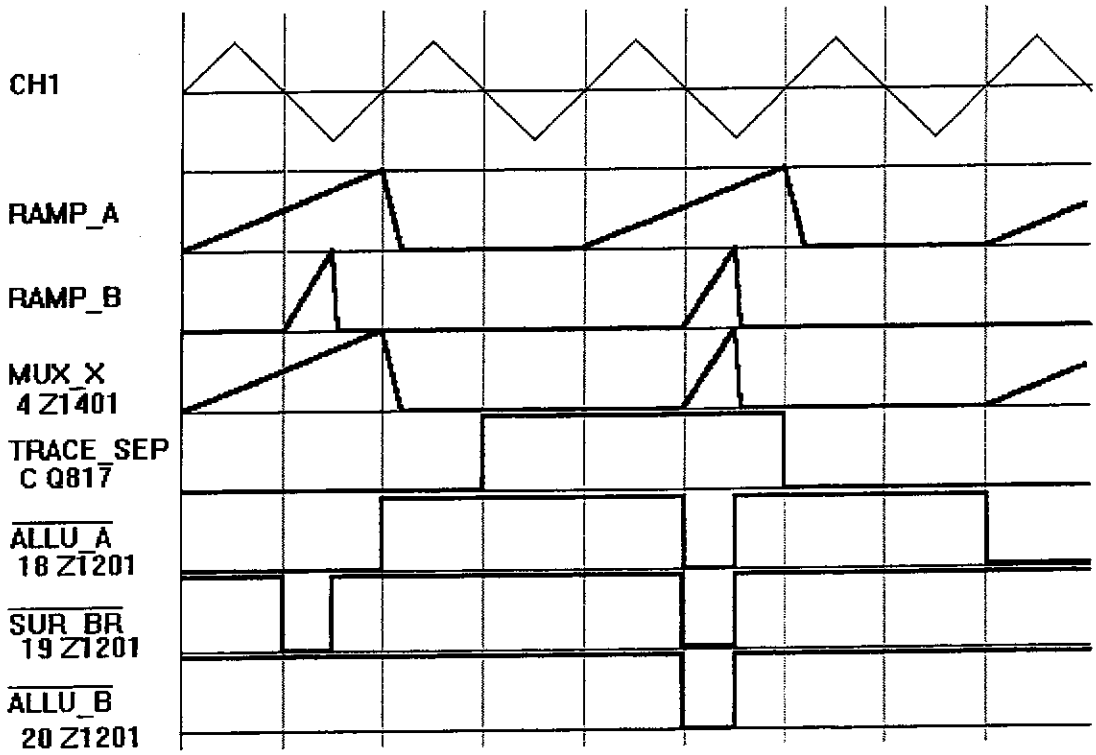
8.1 THEORY OF OPERATION

It's the same saw-tooth generator with a few differences because there is no Hold_off, and no AUTO mode timer.

RAMP B starts when RAMP_A crosses the DELAY level. This is done by Z1108 differential amplifier which act as a level substractor in order to obtain the crossing at the ground potential. Z1109 is a zero crossing unlinear amplifier, Q111, Q1110 and Q1109 is the zero crossing comparator. A low level on VALID_TBB enable this circuit. Z1004 is the time base B triggering flip flop and Z1005 (8,9) the ramp state flip flop.

AUTO_SET use Time base B to measure the signal period and then choose the right time base A speed. This is done with a constant DELAY defined by R1136 & R1135 and the SPDT Z1102(1.2.15). So during AUTOSET operation, RAMP_A is set to a low amplitude and time base B is in B TRIG mode. If any period shorter than a predifine value occurs, output 8 of Z1105 goes low and then transmit the result to the front panel µP Z1701.

8.2 WAVEFORMS OF DUAL TIME BASE : MODE A ALT B



8.3 PROGRAMMATION TABLE

T/DIV B	VIT LNT B	BOND RB	UB2	UB1	UB0
100ms	T	T	F	F	T
50ms	T	T	F	T	F
20ms	T	T	F	T	T
10ms	T	T	T	F	F
5ms	T	T	T	F	T
2ms	T	F	F	F	F
1ms	T	F	F	F	T
0.5ms	T	F	F	T	F
0.2ms	T	F	F	T	T
100µs	T	F	T	F	F
50µs	T	F	T	F	T
20µs	F	T	F	T	T
10µs	F	T	T	F	F
5µs	F	T	T	F	T
2µs	F	F	F	F	F
1µs	F	F	F	F	T
0.5µs	F	F	F	T	F
0.2µs	F	F	F	T	T
100ns	F	F	T	F	F
50ns	F	F	T	F	T

9. LOGIC CONTROLS - sheet 12/19 - See Annex 2

Z1201 is the center of the system it contains the following functions:
Beam erasing and brighting
Alternate clock
Time base output multiplexing
Read-out erasing

9.1 LIST OF THE DIFFERENTS I/O

_EFFNUM	:	erase signal for the digital memory OX8620/OX8627
RBA	:	RAMP_A return
RBB	:	RAMP_B return
TBA_SEULE	:	Time base command for single T.B.A operation
TBB_SEULE	:	Time base command for single T.B.B operation
_VAL_D	:	Command of the switch between analog and digital mode
EFF_PAV	:	software beam erasing
CHOP	:	enable vertical SHOP mode
_VISU_CH2	:	enable CH2 to be displayed on the CRT
_VISU_CH1	:	enable CH1 to be displayed on the CRT
PRE_CH1	:	enable SYNC source on CH1
PRE_CH2	:	enable SYNC source on CH2
RESETB	:	main trigger signal for digital memory card
CRENEAUB	:	delayed trigger signal for digital memory card
TRIG_D	:	not use
SYNC_NUM	:	multiplexed trigger for digital memory card
VAL_PRE_SYNC1	:	real time command of sync CH1

VAL_PRE_SYNC2	:	real time command of sync CH2
VALID_CH1	:	real time command of CH1
VALID_CH2	:	real time command of CH2
MIX_XA	:	real time command of TBA to X MIXING
_MIX_XB	:	real time command of TBB to X MIXING
_ALLUMMAGE	:	brighting analog command
ANB	:	Enable ANALOG mode switching
NUMB	:	Enable DIGITAL mode switching

9.2 PROGRAMMATION TABLE

SOURCE	/PRE_CH1	/PRE_CH2	Y/LINE_E	SYNC_EXT
CH1	F	T	T	F
CH2	T	F	T	F
CH1 alt CH2	T	T	T	F
LINE	F	F	F	F
EXT	F	T	T	T

10. CRT INTERFACE - sheet 13/19 - See Annex 2

This sheet contains the Y driver last stage Q916, Q915, a 140V power supply for cut-off the CRT beam and the Whenelt drive amplifier and the CRT BIASING glue (right side of the sheet).

140v power supply

Z202 is a multivibrator which drives Q214 switching transistor. When Q206 is ON C244 is charged under VCC110 minus 40v (the 2 zener) and then at OFF state this charge is transfered to C243 VIA R213 + R209 + D212.

lighting system

Collector signal of Q214 is also used as an AC supply for the amplitude modulation / demodulation system used to transmit Whenelt signal trought it's 2.2kV bias. Modulation is done on K_BT as follow: D209 is a postif peak limiting on R215 cut-off potential, and D208 is a negatif peak limiting on the lighting signal W_BT. As a result K_BT is an AC signal which swing between to limit W_BT and CUT_OFF Than K_BT is transmited to D210/D211 via C210 and W_BT via C209 to D210 A. Finaly the lighting signal is AM demodulated by D211/D210 regarding to the reference KAT constant potential. C209 transmit the HF spectrum of the lighting signal and C210 the BF bias.

11. X AMPLIFIER - sheet 14/19 - See Annex 2

X amplifier have 4 inputs which are:

TBA	:	Time base A
TBB	:	Time base B
SIGNAL_X	:	X in X/Y mode
I_NUMX	:	X for digital mode display (not used on OX 8620)

The three first signals are multiplexed in Z1401. The first stage Q1404/Q1405 is bias controlled CAD_X With is the X position command. CAD_NUMX is an output of the position used in the digital memory PCB.

I_NUMX is first converted into voltage, then amplified and biasing by Q1409/Q1410 and then multiplexed with the rest of X signal via D1402,D1403 / D1405,D1406

Output amplifier is a transimpedance amplifier of (R1438+R1439) 32.5V/mA gain per plates.

12. FRONT PANEL INTERFACE - sheet 15/19 - See Annex 2

It's just a long chain of serial to parrallel registers with some R2R DAC. Serial data are sent by the front panel µP controler then loaded into the registers and then latched.

13. CNA - sheet 16/19 - See Annex 2

Z1601 is an octal serial DAC which is used in the trimming of the OX 8620 - OX 8627

13.1 DACS AFFECTATIONS TABLE

Name	Resolution	Output	Type
Vos Sync1	4 bits	VOS_SYNC1	R2R
Cent X XY	4 bits	Cent X XY	R2R
Vos Sync2	4 bits	VOS_SYNC2	R2R
Vos Sync Ext	4 bits	VOS_SYNC2	R2R
Vos Mux1 >2mV	8 bits	VOS_MUX1	DAC_8.
Vos Mux1 2mV	8 bits	VOS_MUX1	DAC_8.
Vos Mux2 >2mV	8 bits	VOS_MUX2	DAC_8.
Vos Mux2 2mV	8 bits	VOS_MUX2	DAC_8.
Vos Dec2	8 bits	VOS_DEC2	DAC_8.
Vos Dec2 Inv	8 bits	VOS_DEC2	DAC_8.
Vos Dec2 Add	8 bits	VOS_DEC2	DAC_8.
Vos Dec2 Add Inv	8 bits	VOS_DEC2	DAC_8.
Vos Dec2 XY	8 bits	VOS_DEC2	DAC_8.
Vos Dec2 XY Inv	8 bits	VOS_DEC2	DAC_8.
lox speed A	8 bits	RAMP_ADJA	DAC_8.
fast speed A	8 bits	RAMP_ADJA	DAC_8.
low speed B	8 bits	RAMP_ADJB	DAC_8.
fast speed B	8 bits	RAMP_ADJB	DAC_8.
Gain Mux1 >2mV	8 bits	VAR_ADJ1	DAC_8.
Gain Mux1 2mV	8 bits	VAR_ADJ1	DAC_8.
XY Gain Mux1 >2mV	8 bits	VAR_ADJ1	DAC_8.
XY Gain Mux1 2mV	8 bits	VAR_ADJ1	DAC_8.
Gain Mux2 >2mV	8 bits	VAR_ADJ2	DAC_8.
Gain Mux2 2mV	8 bits	VAR_ADJ2	DAC_8.

14. FRONT PANEL - sheet 17/19 to 19/19 - See Annex 2

It is organised around Z1701 80C52 micro controler. All the keys and the encoders are arranged in a matrix form. This matrix is in scrutation mode that is to say port P10 to P17 plus P32 drive columns and P0 to P7 sence the lines and then the right commands are deduced by software.

The commands data are put in a serial form and then transmitted via a serial bus to the serial to parrallel registers of sheet 15/19

Status of the OX 8620 is displayed by LED's display. Lines P10 to P17 drive the columns of the matrix and P20 to P27 drive the matrix lines.

Others functions of the µP :

Generate the calibrator signal
Back_up the current status of the front panel in an E²PROM serial memory at power down.

Others functions of the front panel :

Sources multiplex of the level signal
Supply all the potentiometric commands

NB : E²PROM serial memory also countains OX 8620 calibration data so if you replace the front panel PCB, you should re-adjust OX 8620 or exchange the two E²PROM.

CHAPTER 3 - ANALOG BOARD ADJUSTMENT

1. EQUIPMENT REQUIRED

A calibration Generator (TEKTRONIX CG5001 + SG503)
A BNC/BNC adjustment plug
A Personnal computer with a RS232 port.
The OX 8620 - OX 8627 calibration software program
RS 232 cable - ref.
Calibration software - ref. 8620. ALL.EXE (860/8620/8627).

2. PREPARATION

Turn on the test equipment and allow 30-minute warm-up before starting the procedure.
Turn off the oscilloscope.
Remove the upper box.
Connect the OX 8620 / OX 8627 RS232 interface.
Turn on the instrument.
Execute the OX 8620 / OX 8627 calibration software

3. ADJUSTMENTS

If necessary load the software '*Gain mux CH1 (calibre > 2mV/Div* control with digital value 0xC0 and '*Centrage position CH2*' with 0x7F.

3.1 CUT OFF ADJUSTMENT

Set :	CH1 coupling	GND
	CH2 coupling	GND
	Horizontal mode	DLY
	Trigger mode	AUTO
	Time base A	100mS/Div
	Time base B	100mS/Div

Turn the front panel potentiometer 'INTENSITY' to its left position.
Adjust potentiometer **R215** for minimum brightness display.

3.2 TRACE ROTATION ADJUSTMENT

Adjust the potentiometer **R1704** to align the traces to the horizontal graticules lines.

3.3 GEOMETRY / ASTIGMATISM ADJUSTMENT

Set :

CH1 coupling	AC
CH1 VOLT/DIV	20mV
Vertical mode	CH1
Horizontal mode	Normal
Time base A	20µS/Div

Input a 1MHz square signal on CH1.
Adjust potentiometer **R261** and FOCUS front panel potentiometer for most uniform focus over the entire displayed pattern.

3.4 CH1 AC/DC GAIN ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	20mV
Vertical mode	CH1
Horizontal mode	Normal
Time base A	0.2mS/Div

Input a 1KHz square signal on CH1.
Adjust potentiometer **R346** to bring the square signal edge overshoot to the plateau.

3.5 CH1 GAIN ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	20mV
Vertical mode	CH1
Horizontal mode	Normal
Time base A	20µS/Div

Input a 120mV 10KHz square signal on CH1.
Adjust potentiometer **R894** for a 6 divisions display.

3.6 CH1 1/10 ATTENUATOR ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	50mV
Vertical mode	CH1
Horizontal mode	Normal
Time base A	10µS/Div

Input a 300mV 10KHz ($tr < 1\mu S$) square signal on CH1.
Adjust variable capacitor **C305** to bring the square signal edge overshoot to the plateau.

3.7 CH1 1/20 ATTENUATOR ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	0.5V
Vertical mode	CH1
Horizontal mode	Normal
Time base A	10µS/Div

Input a 3mV 10KHz (tr < 1µS) square signal on CH1.
Adjust variable capacitor **C312** to bring the square signal edge overshoot to the plateau.

3.8 CH1 1/10 + 1/20 ATTENUATOR ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	1V
Vertical mode	CH1
Horizontal mode	Normal
Time base A	10µS/Div

Input a 6V 10KHz (tr < 1µS) square signal on CH1.
Adjust variable capacitor **C310** to bring the square signal edge overshoot to the plateau.

3.9 CH1 INPUT CAPACITY ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	20mV
Vertical mode	CH1
Horizontal mode	Normal
Time base A	0.2mS/Div

Input a 240mV 1KHz (tr < 1µS) square signal on CH1.
Connect BNC/BNC adjustment plug (attenuator 1/2 compensated) to CH1 input.
Adjust plug compensation capacity to bring the square signal edge overshoot to the plateau.

Set : CH1 VOLT/DIV 50mV

Input a 600mV 1KHz (tr < 1µS) square signal on CH1.
Adjust variable capacitor **C304** to bring the square signal edge overshoot to the plateau.

3.10 CH1 1/10 ATTENUATOR CHECK

Set :

CH1 coupling	DC
CH1 VOLT/DIV	50mV
Vertical mode	CH1
Horizontal mode	Normal
Time base A	10µS/Div

Input a 600mV 10KHz (tr < 1µS) square signal on CH1.
If necessary, adjust variable capacitor **C305** to bring the square signal edge overshoot to the plateau.
Remove the BNC/BNC adjustment plug.

3.11 CH2 AC/DC GAIN ADJUSTMENT

Set :

CH2 coupling	DC
CH2 VOLT/DIV	20mV
Vertical mode	CH2
Horizontal mode	Normal
Time base A	0.2mS/Div

Input a 1KHz square signal on CH2.
Adjust potentiometer **R439** to bring the square signal edge overshoot to the plateau.

3.12 MUX CH2 GAIN ADJUSTMENT

Software control 'Gain mux CH2 (calibre > 2mV/Div)'

Set :

CH2 coupling	DC
CH2 VOLT/DIV	20mV
Vertical mode	CH2
Horizontal mode	Normal
Time base A	0.2mS/Div

Input a 120mV 10KHz square signal on CH2.
Use software adjustment for a 6 divisions display.

3.13 CH2 1/10 ATTENUATOR ADJUSTMENT

Set :

CH2 coupling	DC
CH2 VOLT/DIV	50mV
Vertical mode	CH2
Horizontal mode	Normal
Time base A	10µS/Div

Input a 300mV 10KHz (tr < 1µS) square signal on CH2.
Adjust variable capacitor **C405** to bring the square signal edge overshoot to the plateau.

3.14 CH2 1/20 ATTENUATOR ADJUSTMENT

Set :

CH2 coupling	DC
CH2 VOLT/DIV	0.5V
Vertical mode	CH2
Horizontal mode	Normal
Time base A	10µS/Div

Input a 3V 10KHz (tr < 1µS) square signal on CH2.
Adjust variable capacitor **C412** to bring the square signal edge overshoot to the plateau.

3.15 CH2 1/10 + 1/20 ATTENUATOR ADJUSTMENT

Set :

CH2 coupling	DC
CH2 VOLT/DIV	1V
Vertical mode	CH2
Horizontal mode	Normal
Time base A	10µS/Div

Input a 6V 10KHz (tr < 1µS) square signal on CH1.
Adjust variable capacitor **C410** to bring the square signal edge overshoot to the plateau.

3.16 CH2 INPUT CAPACITY ADJUSTMENT

Set :

CH2 coupling	DC
CH2 VOLT/DIV	20mV
Vertical mode	CH2
Horizontal mode	Normal
Time base A	0.2mS/Div

Input a 240mV 1KHz (tr < 1µS) square signal on CH2.
Connect BNC/BNC adjustment plug (attenuator 1/2 compensated) to CH2 input.
Adjust plug compensation capacity to bring the square signal edge overshoot to the plateau.

Set : CH2 VOLT/DIV 50mV

Input a 600mV 1KHz (tr < 1µS) square signal on CH2.
Adjust variable capacitor **C404** to bring the square signal edge overshoot to the plateau.

3.17 CH2 1/10 ATTENUATOR CHECK

Set :	CH2 coupling	DC
	CH2 VOLT/DIV	50mV
	Vertical mode	CH2
	Horizontal mode	Normal
	Time base A	10µS/Div

Input a 600mV 10KHz (tr < 1µS) square signal on CH1.
If necessary, adjust variable capacitor **C305** to bring the square signal edge overshoot to the plateau.
Remove the BNC/BNC adjustment plug.

3.18 MUX CH1 GAIN ADJUSTMENT ON 2MV/DIV RANGE

Software control 'Gain mux CH1 (calibre 2mV/Div)'

Set :	CH1 coupling	DC
	CH1 VOLT/DIV	2mV
	Vertical mode	CH1
	Horizontal mode	Normal
	Time base A	2µS/Div

Input a 12mV 10KHz square signal on CH1.
Use software adjustment for a 6 divisions display.

3.19 MUX CH2 GAIN ADJUSTMENT ON 2MV/DIV RANGE

Software control 'Gain mux CH2 (calibre 2mV/Div)

Set :	CH2 coupling	DC
	CH2 VOLT/DIV	2mV
	Vertical mode	CH2
	Horizontal mode	Normal
	Time base A	2µS/Div

Input a 12mV 10KHz square signal on CH2.
Use software adjustment for a 6 divisions display.

3.20 CH1 MUX OFFSET COMPENSATION

Software control 'Offset mux CH1 (calibre > 2mV/Div)

Set :	CH1 coupling	AC
	CH1 VOLT/DIV	5mV
	Vertical mode	CH1
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH1 input.
Turn CH1 vertical gain potentiometer GVAR1 all the way through from the left to right stop.
Use software adjustment so that vertical movement of the beam is at its minimum when the GVAR1 potentiometer is turned .

3.21 CH1 MUX OFFSET COMPENSATION ON 2MV/DIV RANGE

Software control 'Offset mux CH1 (calibre 2mV/Div)'

Set :	CH1 coupling	AC
	Vertical mode	CH1
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH1 input.
Switch the 5mV and 2mV/Div CH1 ranges.
Use software adjustment so that vertical movement cannot be seen when the two ranges are switched.

3.22 CH2 MUX OFFSET COMPENSATION

Software control 'Offset mux CH2 (calibre > 2mV/Div)'

Set :	CH2 coupling	AC
	CH2 VOLT/DIV	5mV
	Vertical mode	CH2
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH2 input.
Turn CH2 vertical gain potentiometer GVAR2 all the way through from the left to right stop.
Use software adjustment so that vertical movement of the beam is at its minimum when the GVAR2 potentiometer is turned .

3.23 CH1 MUX OFFSET COMPENSATION ON 2MV/DIV RANGE

Software control 'Offset mux CH2 (calibre 2mV/Div)'

Set :	CH2 coupling	AC
	Vertical mode	CH2
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH2 input.
Switch the 5mV and 2mV/Div CH2 ranges.
Use software adjustment so that vertical movement cannot be seen when the two ranges are switched.

3.24 CH2 OFFSET INVERT COMPENSATION

Software control 'Offset -CH2'

Set :		
	CH2 coupling	GND
	CH2 VOLT/DIV	1V
	Vertical mode	CH2
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH2 input.
Use software adjustment so that vertical movement cannot be seen when the inversion control (-CH2) is set.

3.25 ADD MODE OFFSET COMPENSATION

Software control 'Offset CH2 mode ADD'

Set :		
	CH1 coupling	GND
	CH2 coupling	GND
	CH2 invert	OFF
	CH1 VOLT/DIV	1V
	CH2 VOLT/DIV	1V
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH1 input.
No signal on CH2 input.
Oscilloscope in vertical mode ALT.
CH1 and CH2 beam on the horizontal mid-line of the screen.
Switch scope from ALT mode to ADD.
Use software adjustment to cancel the vertical offset.

3.26 XY MODE OFFSET COMPENSATION

Software control 'Offset CH2 mode XY'

Set :		
	CH1 coupling	GND
	CH2 coupling	GND
	CH2 invert	OFF
	CH1 VOLT/DIV	1V
	CH2 VOLT/DIV	1V
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH1 input.
No signal on CH2 input.
Oscilloscope in vertical mode ALT.
CH1 and CH2 beam on the horizontal mid-line of the screen.
Switch scope from ALT mode to XY.
Use software adjustment to cancel the vertical offset.

3.27 X-Y MODE OFFSET COMPENSATION

Software control 'Offset -CH2 mode XY'

Set :	CH1 coupling	GND
	CH2 coupling	GND
	CH2 invert	ON
	CH1 VOLT/DIV	1V
	CH2 VOLT/DIV	1V
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH1 input.
No signal on CH2 input.
Oscilloscope in vertical mode ALT.
CH1 and CH2 beam on the horizontal mid-line of the screen.
Switch scope from ALT mode to XY.
Use software adjustment to cancel the vertical offset.

3.28 CH1-CH2 OFFSET COMPENSATION

Software control 'Offset -CH2 mode ADD'

Set :	CH1 coupling	GND
	CH2 coupling	GND
	CH2 invert	ON
	CH1 VOLT/DIV	1V
	CH2 VOLT/DIV	1V
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

No signal on CH1 input.
No signal on CH2 input.
Oscilloscope in vertical mode ALT.
CH1 and CH2 beam on the horizontal mid-line of the screen.
Switch scope from ALT mode to ADD.
Use software adjustment to cancel the vertical offset.

3.29 HORIZONTAL GAIN ADJUSTMENT

Set :	CH1 coupling	GND
	CH1 VOLT/DIV	5V
	Vertical mode	CH1
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

Adjust potentiometer **R1410** to obtain a horizontal beam of 10 div + 3 mm.

3.30 XY MODE HORIZONTAL OFFSET COMPENSATION

Software control 'Cadrage X mode XY'

Set :	CH1 coupling	GND
	CH2 coupling	GND
	CH1 VOLT/DIV	5V
	CH2 VOLT/DIV	5V
	Vertical mode	ALT
	Horizontal mode	Normal
	Time base mode	AUTO
	Time base A	50µS/Div

Set the beam start on the first vertical line of the screen with the X position potentiometer.
CH1 and CH2 beam on the horizontal mid-line of the screen.
Switch scope from ALT mode to XY.
Use software adjustment to cancel the horizontal offset.

3.31 X GAIN ADJUSTMENT IN MODE XY

Software control 'Gain mux CH1 (XY,calibre > 2mV/Div)'

Set :	CH1 coupling	AC
	CH2 coupling	GND
	CH1 VOLT/DIV	20mV
	CH2 VOLT/DIV	5V
	Vertical mode	XY

Input a 120mV 1KHz square signal on CH1.
Use software adjustment for a 6 divisions display.

3.32 X GAIN ADJUSTMENT IN MODE XY ON 2MV/DIV RANGE

Software control 'Gain mux CH1 (XY,calibre 2mV/Div)'

Set :	CH1 coupling	AC
	CH2 coupling	GND
	CH1 VOLT/DIV	2mV
	CH2 VOLT/DIV	5V
	Vertical mode	XY

Input a 12mV 1KHz square signal on CH1.
Use software adjustment for a 6 divisions display.

3.33 TIME BASE A ADJUSTMENT

Set :	CH1 coupling	DC
	CH1 VOLT/DIV	0.5V
	Vertical mode	CH1
	Horizontal mode	Normal

3.33.1 Low speed time base A adjustment

Software control 'Reglage vitesse lente BDTA'

Set : Time base A 50µS/Div

Input a 50µS/Div time base calibration signal on CH1 input.
Use software adjustment so as to obtain a calibrator time signal per horizontal division on the tube.

3.33.2 High speed time base A adjustment

Software control 'Reglage vitesse rapide BDTA'

Set : Time base A 20µS/Div

Input a 20µS/Div time base calibration signal on CH1 input.
Use software adjustment so as to obtain a calibrator time signal per horizontal division on the tube.

3.33.3 Low speed time base B adjustment

Software control 'Reglage vitesse lente BDTB'

Set :

Time base A	50µS/Div
Horizontal mode	DLY
Time base B	50µS/Div

Input a 50µS/Div time base calibration signal on CH1 input.
Use software adjustment so as to obtain a calibrator time signal per horizontal division on the tube.

3.33.4 High speed time base B adjustment

Software control 'Reglage vitesse rapidee BDTB'

Set :

Time base A	20µS/Div
Horizontal mode	DLY
Time base B	20µS/Div

Input a 20µS/Div time base calibration signal on CH1 input.
Use software adjustment so as to obtain a calibrator time signal per horizontal division on the tube.

3.34 *10 HORIZONTAL GAIN ADJUSTMENT

Set :

CH1 coupling	DC
CH1 VOLT/DIV	0.5V
Vertical mode	CH1
Horizontal mode	Normal
Time base A	50µS/Div
Horizontal *10	ON

Input a 5µS/Div time base calibration signal on CH1 input.
Adjust **R1413** so as to obtain a calibrator time signal per horizontal division on the tube.

3.35 CH1 TRIGGERING SOURCE OFFSET COMPENSATION

Software control 'Offset synchro CH1'

Set :

CH1 coupling	AC
CH1 VOLT/DIV	0.2V
Vertical mode	CH1
Trigger source	CH1
Time base A	5µS/Div

Input a 1.2V 50KHz sinewave signal to CH1.
Synchronize signal to about 0V using level potentiometer.
Switch AC/DC triggering filters. Use software adjustment until sweep start vertical movement cannot be noticed when switching on the two filters.

3.36 CH2 TRIGGERING SOURCE OFFSET COMPENSATION

Software control 'Offset synchro CH2'

Set :

CH2 coupling	AC
CH2 VOLT/DIV	0.2V
Vertical mode	CH2
Trigger source	CH2
Time base A	5µS/Div

Input a 1.2V 50KHz sinewave signal to CH2.
Synchronize signal to about 0V using level potentiometer.
Switch AC/DC triggering filters.
Use software adjustment until sweep start vertical movement cannot be noticed when switching on the two filters.

3.37 EXT TRIGGERING SOURCE OFFSET COMPENSATION

Software control 'Offset synchro EXT'

Set :

CH2 coupling	AC
CH2 VOLT/DIV	0.2V
Vertical mode	CH2
Trigger source	EXT
Time base A	5µS/Div

Input a 1.2V 50KHz sinewave signal to CH2 and EXT input at the same time.
Synchronize signal to about 0V using level potentiometer.
Switch AC/DC triggering filters.
Use software adjustment until sweep start vertical movement cannot be noticed when switching on the two filters.

3.38 CH1 & CH2 INPUTS BANDWIDTH ADJUSTMENTS

Set :

CH1 coupling	AC
CH2 coupling	AC
CH1 VOLT/DIV	50mV
CH2 VOLT/DIV	50mV
Vertical mode	ALT
Trigger source	CH1
Time base A	0.1µS/Div

Connect a 50 ohm adapting load to CH1 input.
Connect a fast rise output of a calibration generator ($300mV_{pp}$.Tr < 1nS) to the CH1 input connector.
Adjust C509 ...
Set : Horizontal *10 expansion ON

Set *10 expansion on
Connect a 50 ohm adapting load to CH2 input.

3.39 CH1 & CH2 INPUTS BANDWIDTH CHECK

Set : CH1 VOLT/DIV 5mV
CH2 VOLT/DIV 5mV

Check for input bandwidth about 120mhz

CHAPTER 4 - DIGITAL BOARD DESCRIPTION

1. DIGITAL ACQUISITION BOARD

This document describes how the digital board works.Refer to the electrical scheme as needed while reading the following description.

1.1. SIMPLIFIED BLOCK DIAGRAM

Cf. : Figure 1 page 52

1.2. SYSTEM PROCESSOR- Z101 sheet 1 - See Annex 3

The digital conversion board uses a highly integrated 16/32 central processing unit.
This is the SCC68070 from PHILIPS components. It is fully software compatible with the 68000.
Like the 68000 bus, the 68070 external bus has 23 non-multiplexed address lines and 16 data lines with a similar set of control lines.
The µP is driven by an external 19.6608 MHz quartz (Y100) which is divided by 2 internally.The internal clock signal is available at pin 29.
The system processor integrates a serial interface (UART), a 2-channel DMA controller, and two 16-bit timer.

cf. : Figure 2 : Read/Write timing
Figure 3 : 68070 Pin assignments
Figure 4-5-6 : 68070 Signal descriptions

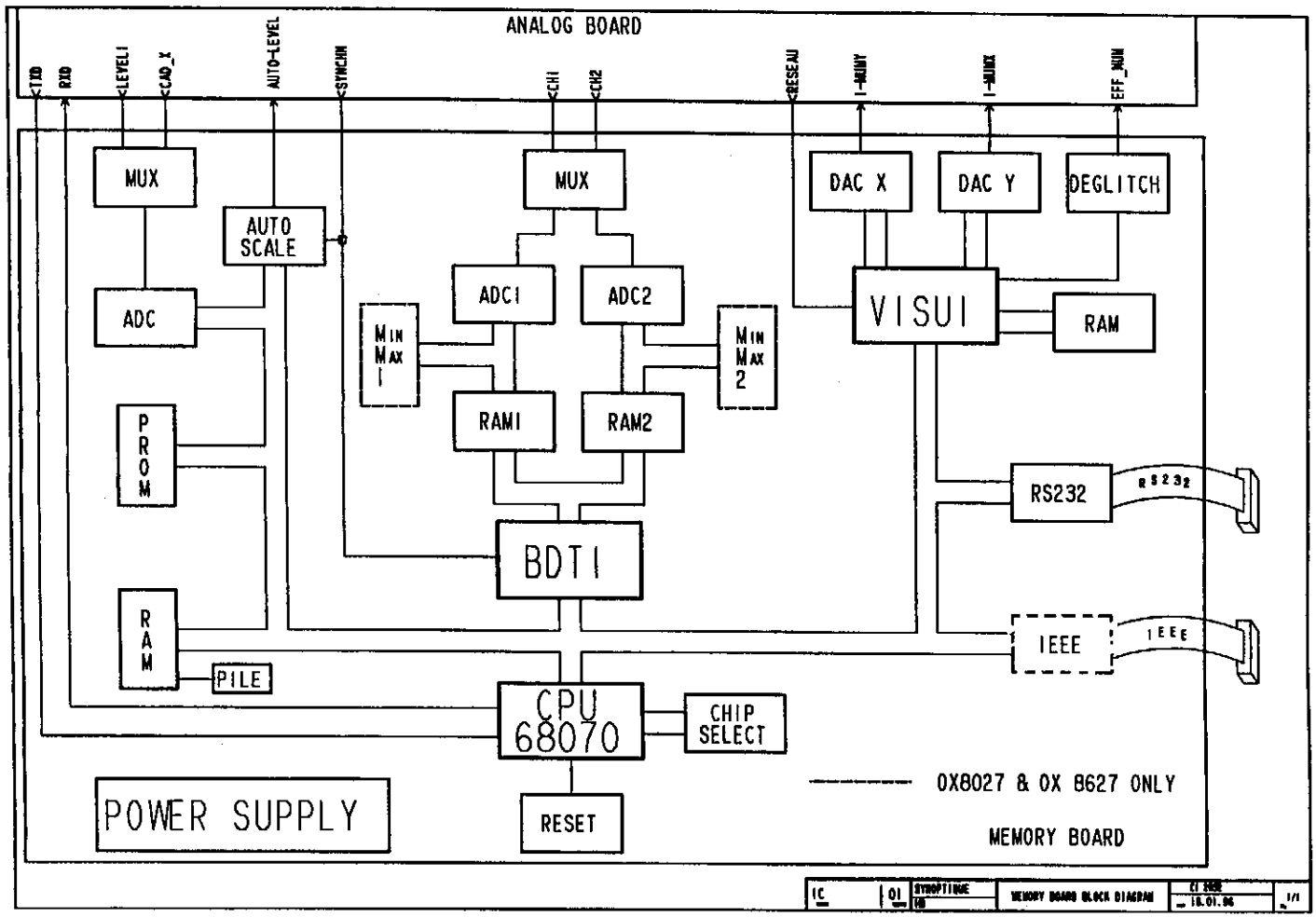


Figure 1 - SIMPLIFIED BLOC DIAGRAM

Figure 2 - READ / WRITE TIMING

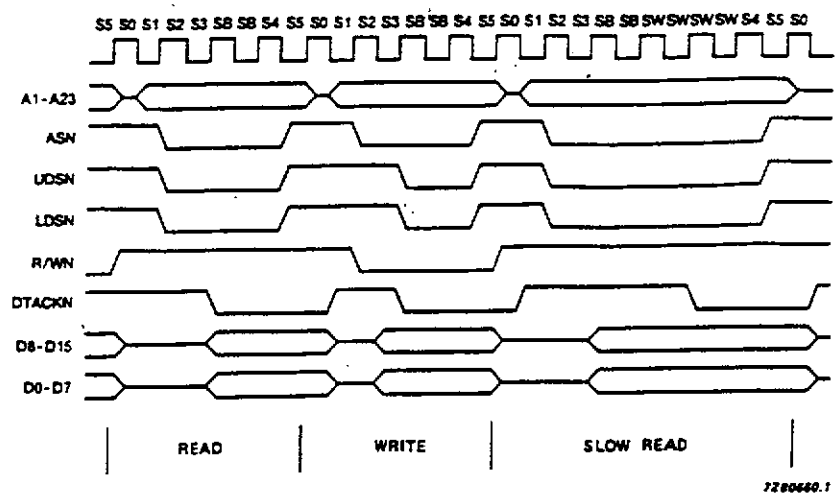


Fig. 2.5 Read and write cycle timing

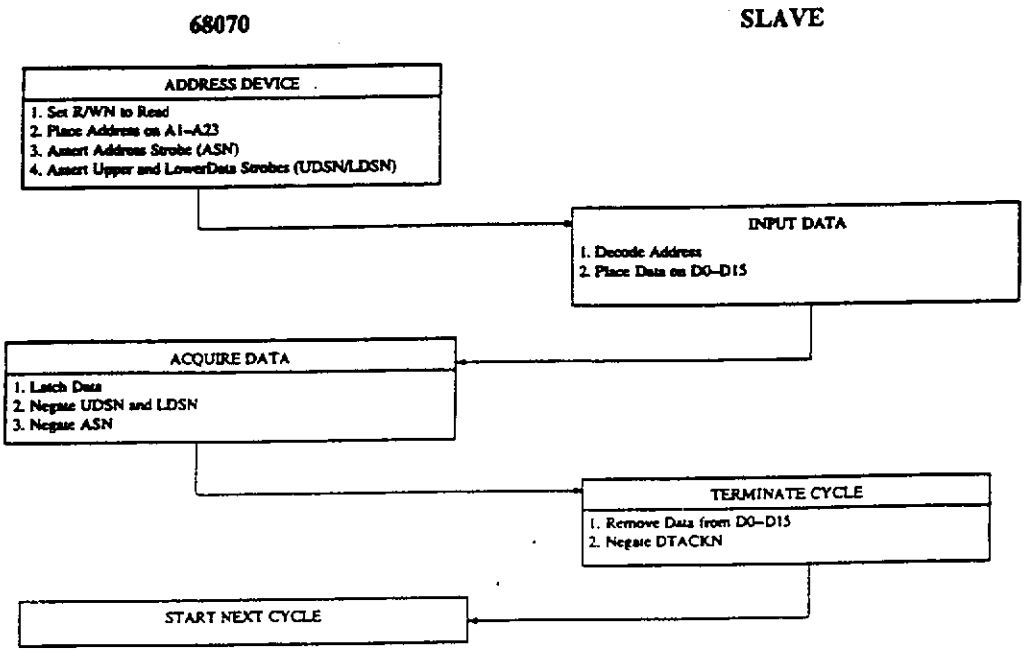


Fig. 2.6 Word read cycle flowchart

Figure 3 - 68070 PIN ASSIGNMENTS

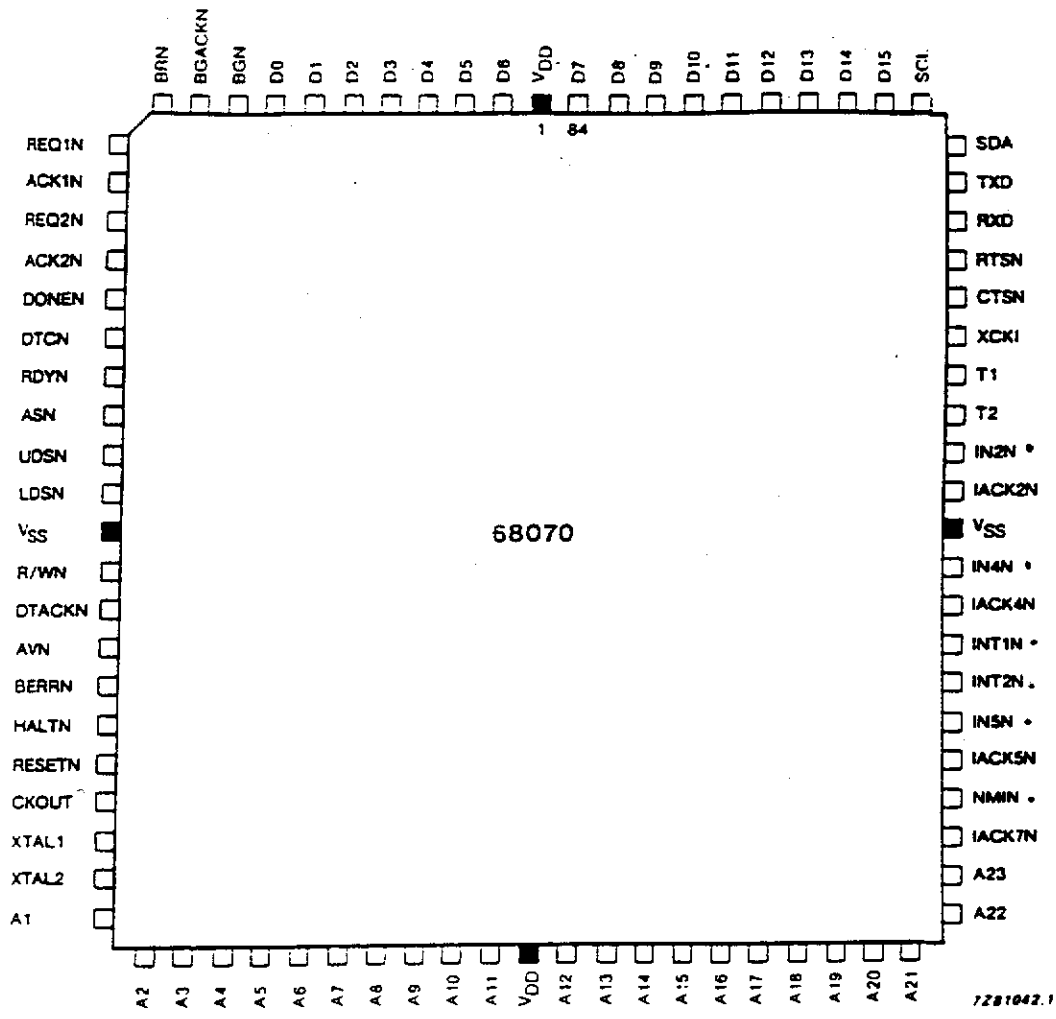


Fig.2 Pinning diagram for PLCC84.

Figure 4 - 68070 SIGNAL DESCRIPTIONS

Signal description (PLCC84)

MNEMONIC	TYPE	PIN NO.	FUNCTION
A1 to A23	O	32-42, 44-55	**Address bus** (active HIGH, 3-state). For direct addressing of 16 Mbytes of memory.
D0 to D15	I/O	8-2, 84-76	**Data bus** (active HIGH, 3-state, bidirectional). 16-bit wide.
ASN	O	19	**Address Strobe** (active LOW, 3-state). Indicates a valid address on the bus.
LDSN	O	21	**Lower Data Strobe** (active LOW, 3-state). Indicates that: - For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). - For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O	20	**Upper Data Strobe** (active Low, 3-state). Indicates that: - For a WRITE cycle, the data is valid on the lower half of the data bus (D8 to D15). -For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O	23	**Read** (active HIGH)/**Write** (active LOW). This controls the direction of data flow.
DTACKN	I	24	**Data Transfer Acknowledge** (active LOW). Asserted by the peripheral during CPU or DMA bus cycles when data is either received from or placed on the bus. If not asserted punctually, it causes the CPU or DMA controller to insert wait states.
BRN	I	11	**Bus Request** (active LOW). Asserted by wired-ORed external DMA devices that request bus ownership.
BGN	O	9	**Bus Grant** (active LOW). A daisy chain output that is asserted by the SCC68070 when the bus is granted by the CPU and the DMA does not have a bus request pending.
BGACKN	I/O	10	**Bus Grant Acknowledge** (active LOW, open drain). Asserted by any DMA device (internal or external) that has control of the bus. As long as this line is held LOW externally, the SCC68070 will hold the bus signals in the high impedance state. When BGACKN is released, the SCC68070 will have access to the bus. Interrupts cannot be serviced while BGACKN is held LOW.
RESETN	I/O	28	**Reset** (active LOW, open drain, bidirectional). If asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the Reset instruction resets external hardware.
HALTN	I/O	27	**Halt** (active LOW, open drain, bidirectional). If asserted externally together with RESETN, it causes the SCC68070 to enter the Reset state. If asserted alone, it will cause the CPU or DMA controller to stop after completion of the current bus cycle. If HALTN and BERRN are asserted together, the CPU will complete the current bus cycle, stop operation, and place all 3-state lines in their high impedance state until HALTN and BERRN have been released, and then it will re-run the same bus cycle. BERRN should be released before HALTN. As long as HALTN is held LOW all control signals are inactive and all 3-state lines are placed in their high impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault) the processor drives this line LOW.
BERRN	I/O	26	**Bus Error** (active LOW, open drain). If this line is asserted during a bus cycle, it indicates that there was a fault in the bus cycle access. If asserted together with HALTN, the same bus cycle will re-run after both HALTN and BERRN have been released. If BERRN is asserted alone, the SCC68070 will start bus-error exception processing. BERRN is driven LOW by the SCC68070 when the MMU indicates a bus error.

Source : Philips Components - 16/32- bit Microprocesseur - SCC68070 - Novembre 1990

Figure 5 - 68070 SIGNAL DESCRIPTIONS

MNEMONIC	TYPE	PIN NO.	FUNCTION
INT1N, INT2N	I	61, 60	**Latched interrupt inputs** (active LOW). A LOW level of ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable.
IN2N, IN4N, IN5N	I	66, 63, 59	**Decoded interrupt priority inputs** (active LOW). IN2N has the lower and IN5N has the higher priority.
NMIN	I	57	**Non-maskable interrupt (level 7)** (active LOW). While the other interrupts may be masked (disabled), this interrupt is always enabled.
IACK2N, IACK4N, IACK5N, IACK7N	O	65, 62, 58, 56	**Decoded interrupt acknowledge** (active Low). Asserted during an interrupt acknowledge sequence to indicate to a peripheral that its interrupt request is being serviced.
AVN	I	25	**Autovectored interrupts** (active LOW). If held LOW during the interrupt acknowledge sequence, the processor calculates the appropriate vector from a fixed vector table. If kept HIGH, the peripheral must provide an 8-bit vector number.
V_{DD}	-	1, 43	Supply voltage + 5.0 V nominal.
V_{SS}	-	22, 64	Ground.
XTAL1, XTAL2	I	30, 31	**External crystal inputs.** XTAL1 can be used as a clock input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O	29	**Clock out.** This is the reference from the internal system clock.
REQ1N, REQ2N	I	12, 14	**DMA Request** (active LOW). These are inputs from I/O devices requesting service from the DMA controller and causes it to request control of the bus. In burst mode, the inputs are level sensitive and the DMA controller releases the bus after REQ1N (or REQ2N) becomes active and the current DMA cycle is completed. In cycle-stealing mode, REQ1N or REQ2N inputs are triggered by a negative pulse. This pulse must occur at least one clock cycle before DTCN is asserted to ensure continuous transfer.
ACK1N, ACK2N	O	13, 15	**DMA Request Acknowledge** (active LOW). ACK1N (or ACK2N) is asserted by the DMA controller to indicate that it has acquired the bus and the requested device bus cycle is now beginning. It is active at the beginning of every device cycle together with ASN, and is deactived at the end of every device bus cycle.
RDYN	I	18	**Device Ready** (active LOW). The requesting device asserts RDYN to indicate to the DMA controller that valid data has either been stored or put on the bus. If RDYN remains inactive, it indicates that the data has neither been stored nor put on the bus, causing the DMA controller to insert wait states. RDYN can be held LOW permanently if the device is fast enough, indicating that the device is always ready and so no wait states are required. RDYN is not monitored by Channel 2 in the dual address mode.
DTCN	O	17	**Device Transfer Complete** (active LOW, open drain). In DMA mode DTCN is asserted by the DMA controller to indicate to the device that the requested data transfer is complete. On a write-to-memory operation, it indicates that the data provided by the device has been stored successfully. On a read-from-memory operation, it indicates that the data from memory is present on the data bus and should be latched.
DONEN	I/O	16	**Done** (active LOW, open drain). With DONEN as an output, the DMA controller asserts it simultaneously with the ACK1N (or ACK2N) output to indicate to the device that the transfer count is zero and therefore, the DMA controller's operation is complete. If, as an input, DONEN is asserted by the device before the transfer count reaches zero, it causes the DMA controller to abort the operation and generate an interrupt request (if the interrupts are enabled).

Source : Philips Components - 16/32- bit Microprocesseur - SCC68070 - Novembre 1990

Figure 6 - 68070 SIGNAL DESCRIPTIONS

MNEMONIC	TYPE	PIN NO.	FUNCTION
SCL	I/O	75	**Serial Clock** (open drain). SCL is the clock signal for the I²C-bus operation. It is either driven by the SCC68070 when the I²C interface is in the master mode, or is the clock input if the I²C interface is in the slave mode.
SDA	I/O	74	**Serial Data** (open drain). SDA is the data signal for the I²C-bus.
T1, T2	I/O	68, 67	**Timers 1 and 2** (3-state). These are the I/O signals for the capture timers of channels 1 and 2 respectively. They can be programmed as either outputs for pulses or inputs for count cycles and events.
RXD	I	72	**Receive Data**. RXD is the data input for the UART serial interface.
TXD	O	73	**Transmit Data**. TXD is data output for the UART serial interface.
RTSN	O	71	**Request To Send** (active LOW). This output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN	I	70	**Clear To Send** (active LOW). This input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected together if no control lines are needed.
XCKI	I	69	**External clock**. When selected, XCKI is the clock input for the UART serial interface. This signal can be used either: - to generate special baud rates or, - when a crystal frequency other than 19.6608 MHz is used by the SCC68070, an external clock of 4.9152 MHz (or 9.8304 for 38200 bauds) can be connected to this input to generate the standard baud rates.

Note

The signal descriptions given for the PLCC84 package also apply to the QFP120 package. However, the pinning arrangement for the QFP120 is different, as can be seen in Fig.3.

Source : Philips Components - 16/32- bit Microprocesseur - SCC68070 - Novembre 1990

1.3. SYSTEM PROCESSOR PERIPHERALS

1.3.1. Reset circuit (Z103 sheet 1)

The power-up reset circuit consists in a TL7705 reset controller IC (Z103) and a electrolytic capacitor.When the instrument is first powered up, the reset controller's RESET output is high, holding the system µP reset at pin 28. The reset controller then monitors the power supply voltage at its SENSE input at pin 7. When the supply voltage, at this input, reaches operating tolerance, the reset controller allows an internal current source to begin charging C104 at pin 3.After at least 300mS (time is determined by the 22 µF capacitor), the voltage on C104 triggers an internal comparator in the reset controller and it removes the reset at pin 28 of the system µP by switching RESET low.The reset controller continues to monitor the power supply at its SENSE input.If the power supply drops below operating limits (4.5V during 2µS), the reset controller drives RESET high to reset the system µP, and at the same time, it discharges C104. The normal power-up sequence previously described can then occur when/if the power supply comes back within limits.

R105 inhibits the watchdog circuit .
J101 allows an external switch to be connected and to help you in testing power-up reset problems.

cf. : Figure 7 : Power-up reset timing
Figure 8-9 : System processor reset timing

1.3.2 Memory map

System µP Adress	A23	A22	A21	A20	High byte (UDSN = 0) $D_{(15:8)}$	Low byte (LDSN = 0) $D_{(7:0)}$
000 000 H	0	0	0	0	System ROM (Z301)	System ROM (Z302)
100 000 H	0	0	0	1	System RAM (Z402)	Sytem RAM (Z401)
200 000 H	0	0	1	0		Display RAM (Z802)
300 000 H	0	0	1	1	Acquisition RAM (Z604)	Acquisition RAM (Z605)
400 000 H	0	1	0	0		DUART 68681 (Z1001)
500 000 H	0	1	0	1		GPIB 7210 (Z901)
600 000 H	0	1	1	0		DISPLAY & ACQUISITION CONTROLLERS (Z601 Z801)
700 000 H	0	1	1	1		ADC LEVEL/CADX (Z502)

Figure 7 : POWER-UP RESET TIMING

VCC - RESET

Pin 8 Z103

RESET

Pin 6 Z 103

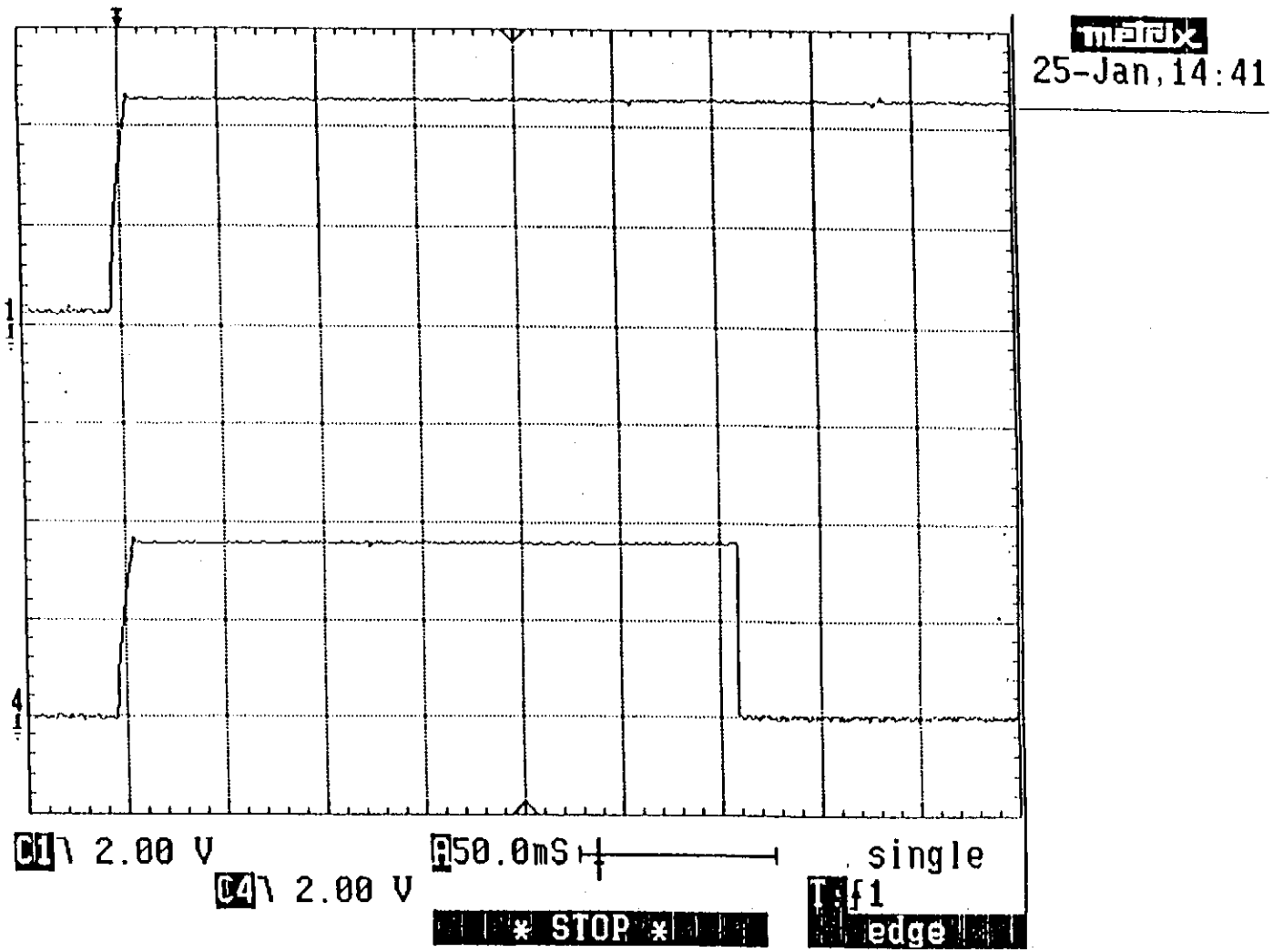
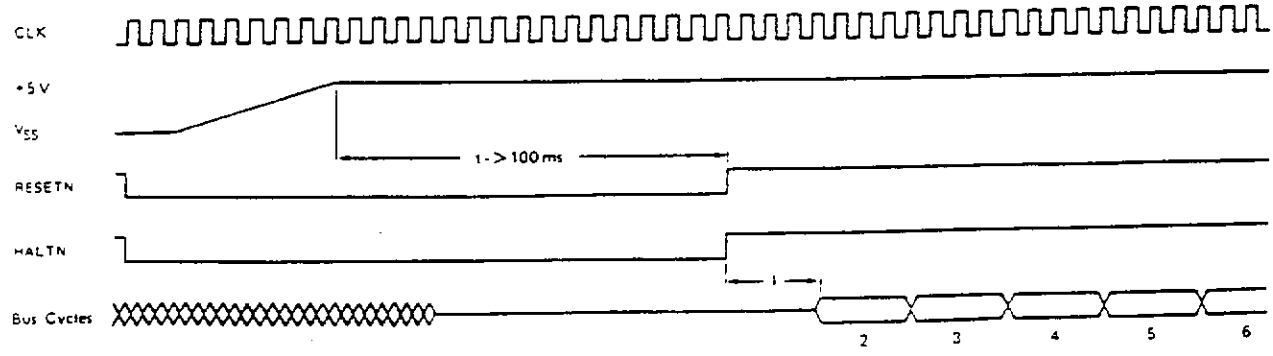


Figure 8 : SYSTEM PROCESSOR RESET TIMING

Reset operation

When the CPU executes a RESET instruction, the RESETN signal is driven LOW for 146 clock cycles to reset internal and external peripherals. The CPU itself is not affected but all on-chip peripherals are reset. When both the RESETN and HALTN signals are driven LOW by an external device, the CPU and on-chip peripherals are reset. The CPU responds by reading the reset vector table entry (vector number zero, address 000000H) and loads it to the Supervisor Stack Pointer (SSP). Vector table entry number one (at address 000004H) is read next and loaded into the Program Counter (PC). The CPU then initializes the Status Register (SR) to an interrupt level of seven and instruction execution is started (see Fig.12).
All 3-state output signals are placed in the high-impedance state for as long as the RESETN and HALTN signals are externally driven. When the RESETN and HALTN signals are released, the CPU will execute 4 read cycles after start-up time, to load the SSP High, SSP Low, PC High and PC Low. Then the first instruction is fetched and executed. The HALTN signal must be driven LOW at the same time as the RESETN signal. The SCC68070 will only start to read the stack and the initial Program Counter after both signals have been released. RESETN should not be released after HALTN.
When V_{DD} is initially applied to the SCC68070, an external RESET must be applied to the RESETN pins for at least 100 ms.



Reset timing.

Source : Philips Components - 16/32-bit microprocessor - SCC68070 - Novembre 1990

Figure 9 : SYSTEM PROCESSOR RESET TIMING

RESETN

Pin 28 Z 101

DTACKN

Pin 24 Z 101

CSEL - B (0)

Pin 24 Z 301