1.3.3. System address decode circuit (Z201 & Z202 sheet 2)

The system address decode circuit uses several of the system address bits, along with other control signals, to connect the system data bus to :

System ROM (Z301 & Z302)	:	Chip select EPROM_B (Z201 pin 19)
System RAM (Z401)	:	Chip select RAMSL_B (Z201 pin 18)
System RAM (Z402)	:	Chip select RAMSU_B (Z201 pin 17)
Acquisition RAM (Z604)	:	Chip select RAMQU1_B (Z201 pin 16)
Acquisition RAM (Z605)	:	Chip select RAMQL2_B (Z201 pin 15)
Display RAM (Z802)	:	Chip select RAMQU1_B (Z201 pin 14)
ADC Level/Cadx (Z502)	:	Chip select ADCLVL_B (Z201 pin 13)
COVIS1 register (Z801)	:	Chip select COVIS1_B (Z202 pin 19)
COVIS2 register (Z801)	:	Chip select COVIS2_B (Z202 pin 18)
COVIS3 register (Z801)	:	Chip select COVIS3_B (Z202 pin 17)
CURS10 register (Z801)	:	Chip select CURS10_B (Z202 pin 16)
BASEDT register (Z601)	:	Chip select BASEDT_B (Z202 pin 15)
RS232 interface (Z1001)	:	Chip select DUART_B (Z202 pin 13)
IEEE interface (Z901)	:	Chip select GPIB_B (Z202 pin 12)

1.3.4. System Rom - Z301 & Z302 - sheet 3/10

The system ROM (read-only memory) is made of two 128K * 8-bit rom devices connected in parallel to form a 128K * 16-bit program memory. The chip enable the pins Z301 and Z302 of the chips are both shorted to ground to reduce access time (no wait-state).

Cf. : Figure 10 : Program fetch with no wait state

2.3.5. System Ram (Z401 & Z402 sheet 4)

The system RAM (random access memory) is made of two 128K * 8-bit memory devices connected in parallel to form a 128K * 16-bit storage memory.The system ram is used for storage of waveform acquisition data,front panel settings,... .
It is nonvolatile RAM . A battery-backup circuit (BT120x) is used to maintain data when power is off.It allows the instrument to power on in the same state it was in when it was turned off.

Figure 10 - PROGRAM FETCH WITH NO WAIT STATE

CSEL - B (0)

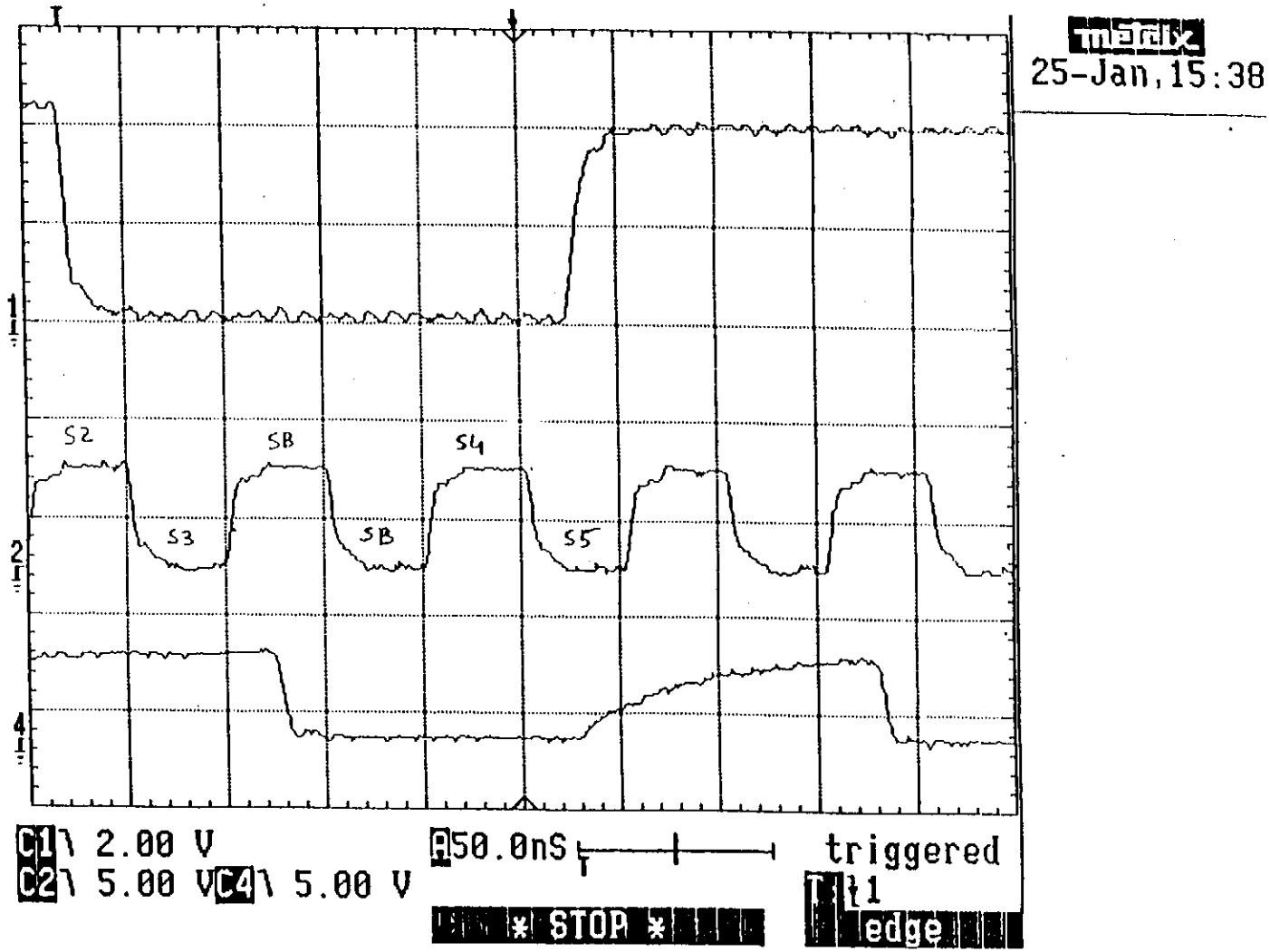
Pin 24 Z 301

CLKCPU

Pin 29 Z 101

DTACKN

Pin 24 Z 301



1.4. ACQUISITION

1.4.1. A/D converters (Z703 & Z704 sheet 7)

Characteristics : 8 bits,20 MHz,monotonic with no missing codes
A/D converter operates at a constant 20 MHz conversion rate.
CR702 provides a 2.5V voltage reference.The magnitude of the analog input VIN is about 1.5V centered around 1.25V.

1.4.2. Time base controller Z601 - sheet 6/19

The time base controller, under direction of the system µP, monitors and controls the acquisition functions. When the pretrigger samples are obtained, the digitization process is started. Samples are counted to store the correct number in the acquisition memory, and the trigger point is properly located in the waveform record.

Record length : 4096 data points for the OX8620. 8192 data points for the OX8627.
The time base controller is driven by an external 40 MHz free running oscillator.

It generates :

- CK1A and CK2A provide the acquisition rate (100 data points per division).
- Two constant phase reversal clocks (20MHzA and 20MHzB) for A/D data conversion rate.
- A 1 MHz clock (CKvisu1) for the display circuit and the level conversion ADC.
- A 2 MHz clock (CKvisu2) for the display circuit.
- A 5 MHz clock for the IEEE interface circuit.

1.4.2.1. Sweep time between 10S/Div and 200mS/Div.

Sweep time between 10S/Div. and 200 ms/Div.
In real time mode, the display is constantly being updated as new data point are available. When the RST7.5 signal from the time base controller goes low,new data point is acquired. A low state is clocked to the Q output of flip-flop Z615 on the falling edge of the RST7.5 signal. That generates an interrupt to the system processor. When the system processor services request, it sets OP(1) low via Z1001 to reset the flip-flop in preparation for the next new data point.

Example : With SEC/DIV control set to 200mS, there is an effective sample rate of 1 sample every 2mS.

Figure 11 : Real time acquisition.Sweep time : 200mS/Div.
Figure 12 : Real time interrupt acknowledge

Figure 11 : Real time acquisition.Sweep time : 200mS/Div.

RST 7.5

Pin 15 Z 601

INT (0)

Pin 5 Z 615

OP (1)

Pin 4 Z 615

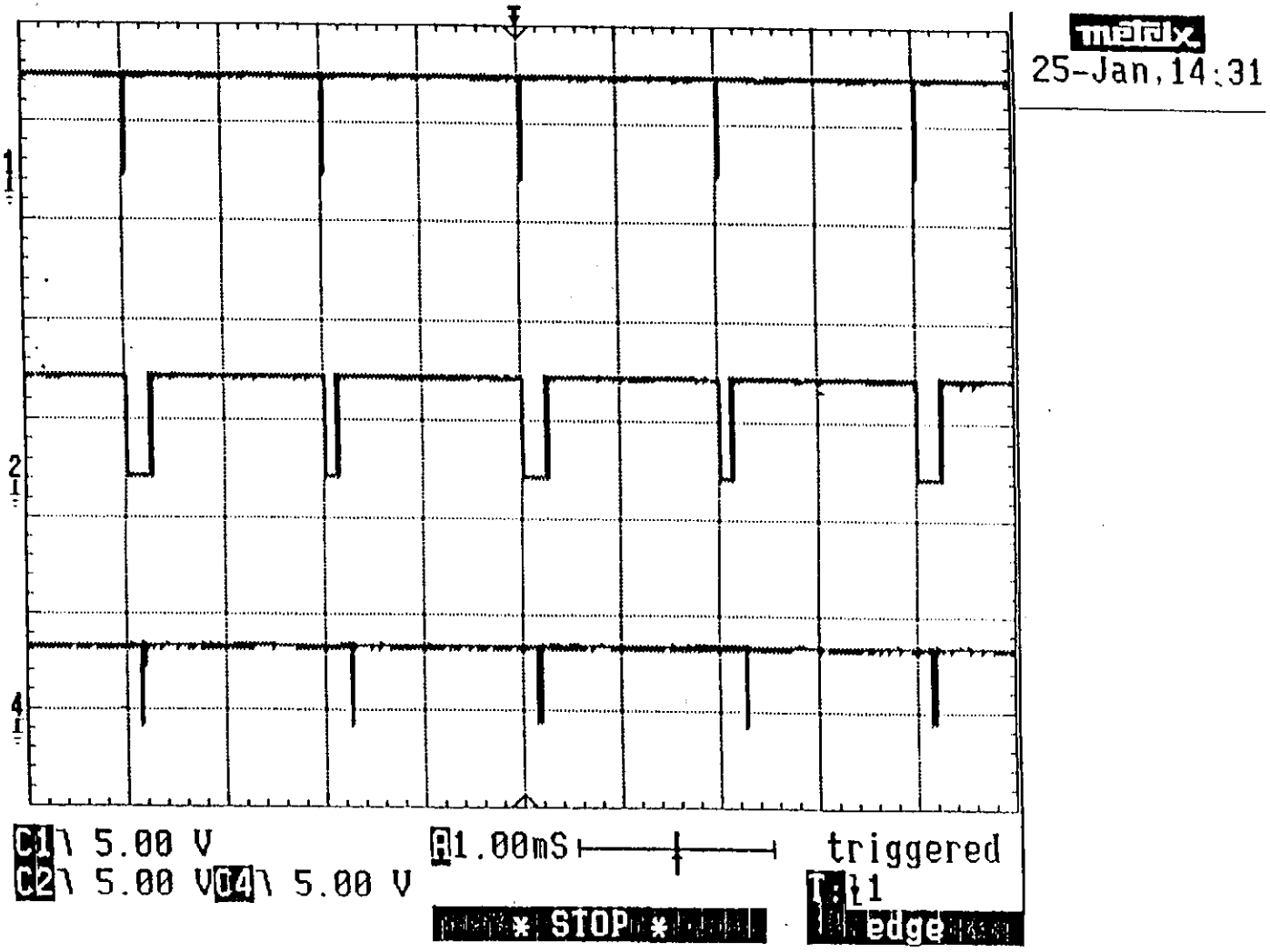


Figure 12 : Real time interrupt acknowledge

RST 7.5

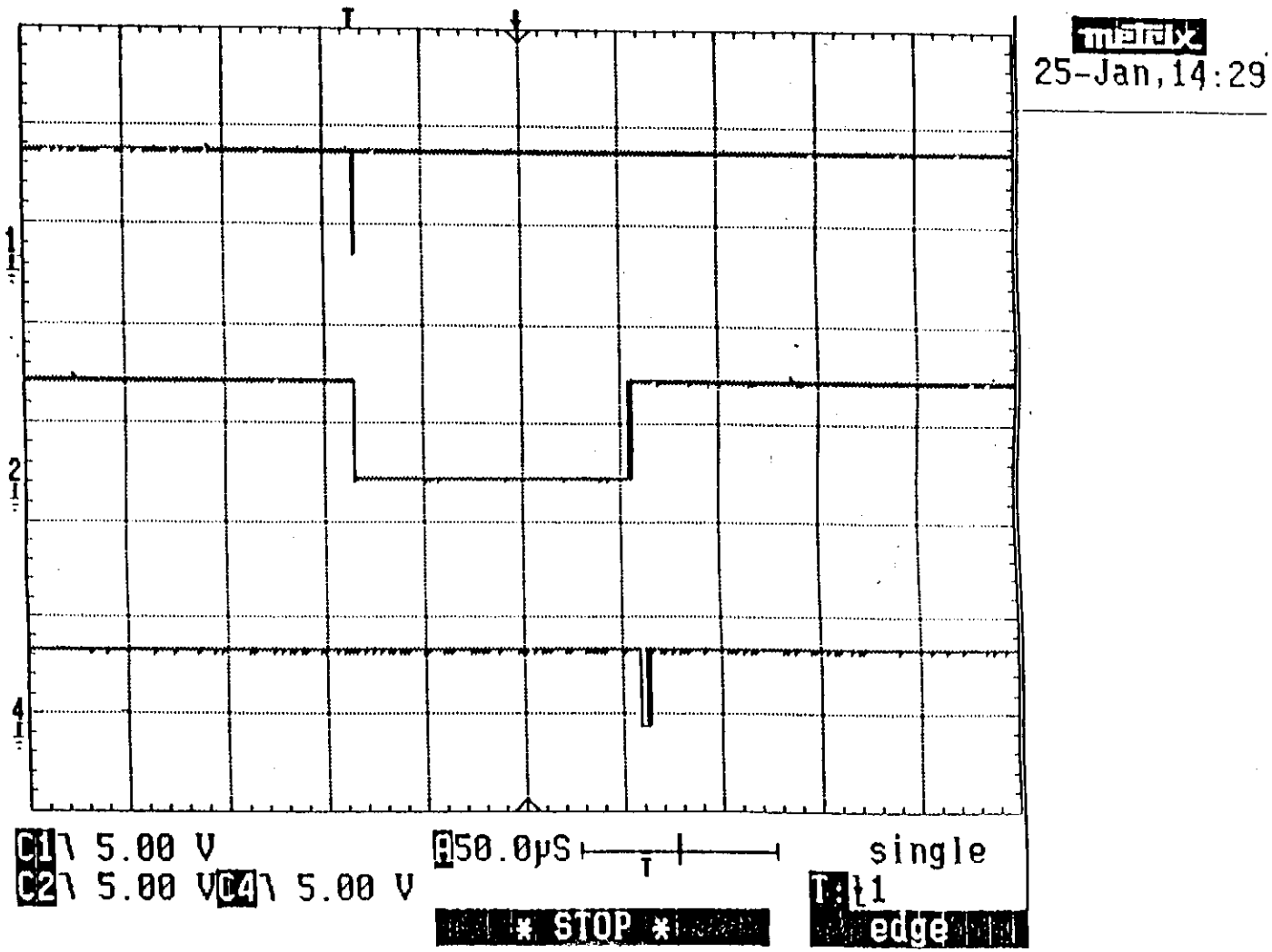
Pin 15 Z 601

INT (0)

Pin 5 Z 615

OP (1)

Pin 4 Z 615



1.4.2.2. Standard mode acquisition

Sweep time between 100mS/Div and 5µS/Div.

The system processor sets the PINGPONG output (Z1101 pin 5) and the PGPGCH2 output (Z1101 pin 6) low.

The input signals (CH1 and CH2) are applied to their corresponding A/D converters for digitization.
A/D converters clocks input are both connected to 20MHzA clock signal (via Z610).

Cf. : Figure 13 : Standard mode acquisition timing.

1.4.2.3. Pingpong mode acquisition

Sweep time : 2µS/Div and lower (Software expansion).

Acquisition rate : 40MS/S for one channel.
The input signal are converted alternately.The A/D converters use a reversal clock input signal.
The system processor sets the PINGPONG output high.

CH1 input signal digitization :
The system processor sets the PGPGCH2 output low.
The input signal CH1 is applied to both A/D converters (via Z702).

CH2 input signal digitization :
The system processor sets the PGPGCH2 output high.
The input signal CH2 is applied to both A/D converters (via Z702).

Cf. : Figure 14 : Pingpong mode acquisition timing.

Figure 13 - Standard mode acquisition timing

(S/DIV : 5µs)

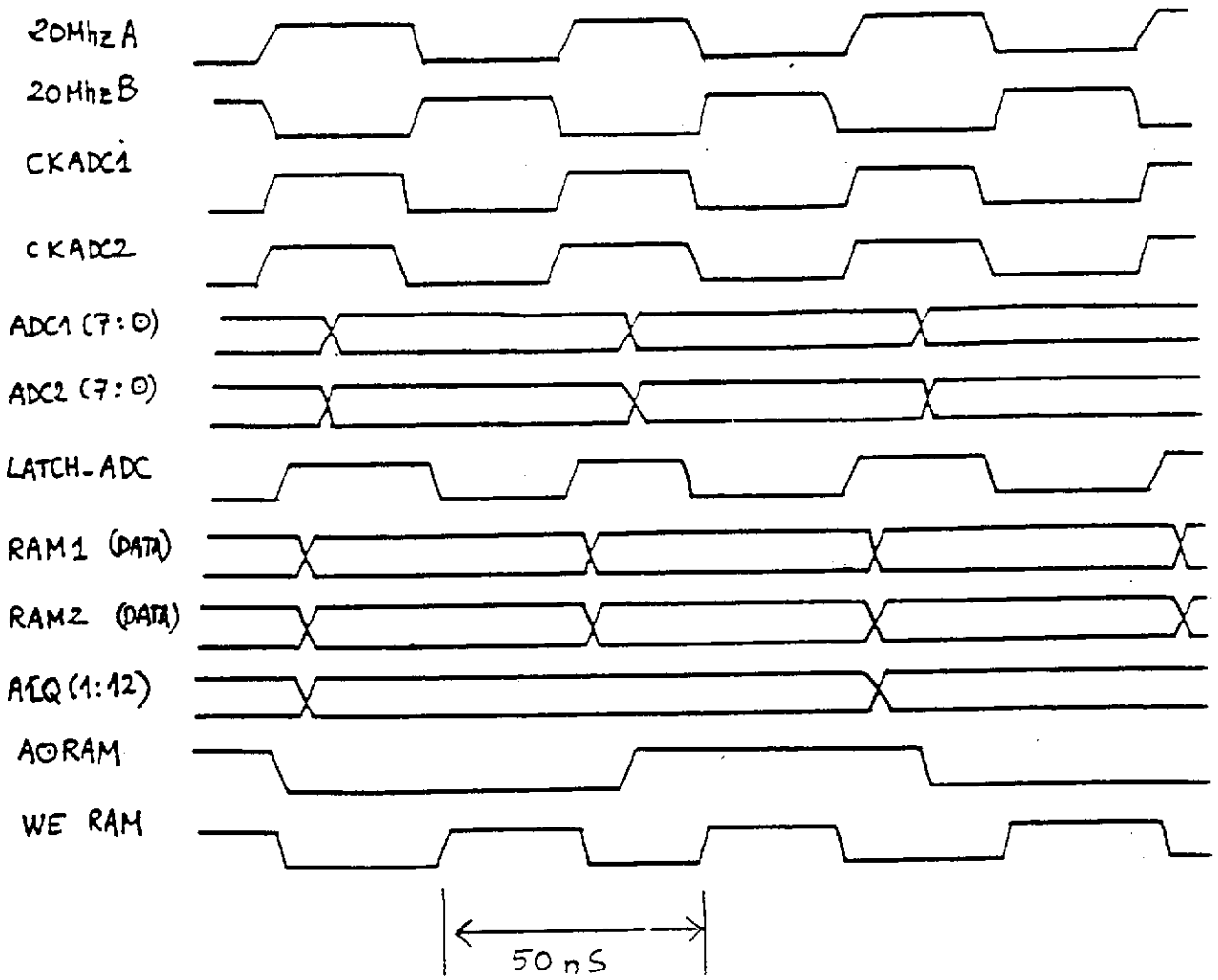
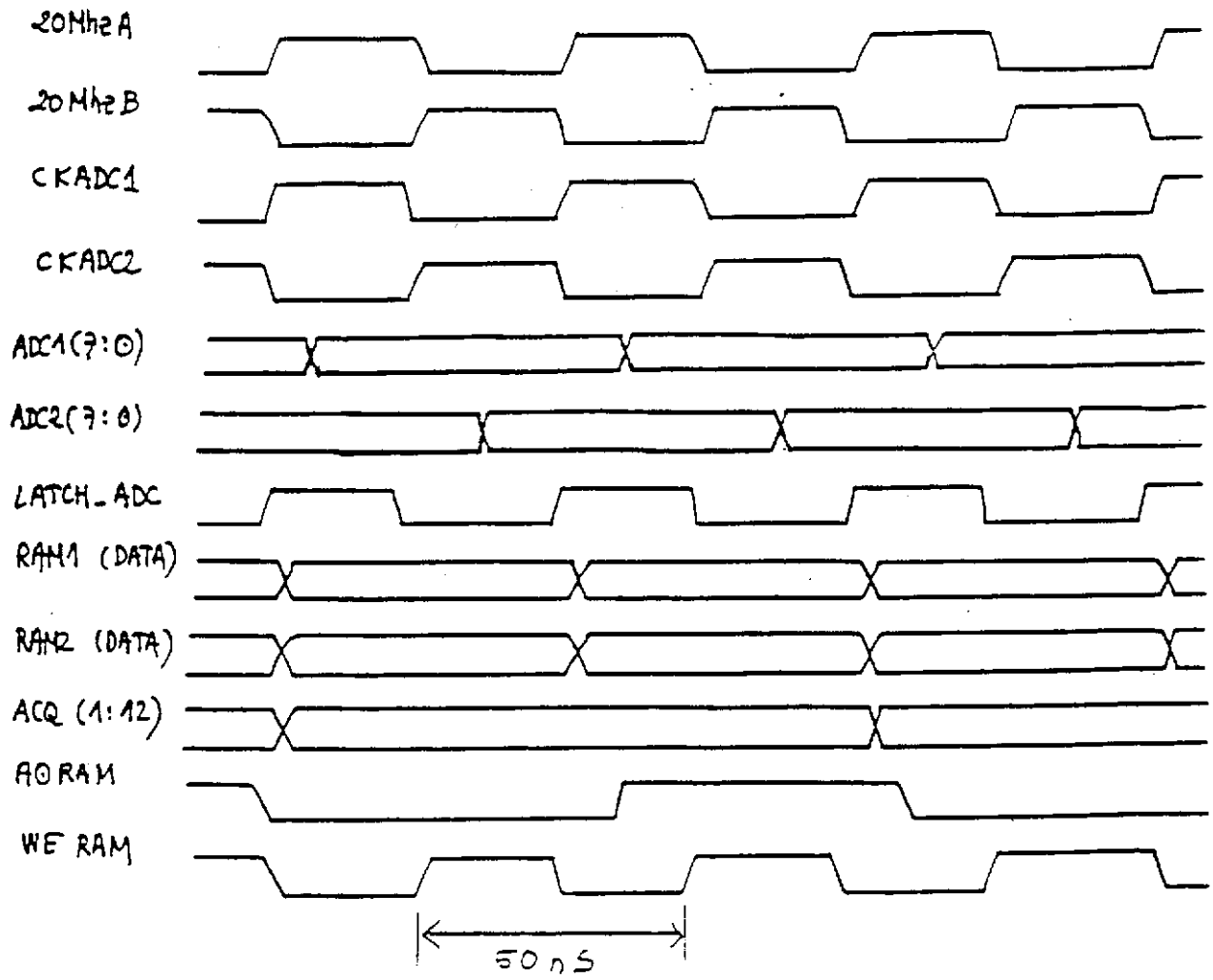


Figure 14 : PINGPONG MODE ACQUISITION TIMING

(S/DIV : 2µs)



1.4.3. Acquisition memories (Z604 & Z605 sheet 6 - See Annex 3

1.4.3.1. Time base controller access

The time base controller (Z601) sets the COMRAM (pin 61) and COMRD_ pin (pin 4) output pins high.

Standard and real time modes acquisition :
The time base controller sets the COM374_ output (Z601 pin 62) low.
The time base controller sets the ENVEL output (Z601 pin 6) high.

Glitch capture mode acquisition :
The time base controller set the COM374_ output (Z601 pin 62) high.
The time base controller set the ENVEL output (Z601 pin 6) low.

1.4.3.1.1. Address bus

An internal counter in time base controller generates the acquisition memory addresses.
Z612 and Z613 synthesize the A0 addresses via Z603.

1.4.3.1.2. Data bus

Z607 and Z608, bidirectional buffers, isolate the system processor data bus from acquisition ram data bus.

Standard and real time modes acquisition :
Z606, unidirectional buffer, connects A/D converter (Z703) to acquisition ram (Z604) data bus.
Z609, unidirectional buffer, connects A/D converter (Z704) to acquisition ram (Z605) data bus.
Z101,Z201,Z104 and Z204 (Glitch capture board), unidirectional buffers, isolates the MINMAX1 and MINMAX2 bus from acquisition ram data bus.(OX8627 only).

Glitch capture mode acquisition : (Ox8627 only)
Z606 and Z609, unidirectional buffers, isolates the A/D converter data bus from acquisition ram data bus.
Z101 (min) and Z104 (max), unidirectional buffers, connects alternately the MINMAX1 bus to acquisition ram (Z604) data bus.
Z201 (min) and Z204 (max), unidirectional buffers, connects alternately the MINMAX2 bus to acquisition ram (Z605) data bus.

1.4.3.1.3. Control signals

The chip select pins of acquisition rams, Z604 and Z605, are both shorted to ground via Z602.
The output enable pins of acquisition rams are both connected to the time base controller output pin COMRD_ .
The time base controller generates the write signal (COMWR_ pin 5) according to the acquisition rate.

1.4.3.2. System processor access

The time base controller sets the COMRAM output low.
The time base controller sets the COM374_ and ENVEL output high.

1.4.3.2.1. Address bus

The system processor address bus is connected to the acquisition ram address bus throughout the time base controller and Z603 (A0).

1.4.3.2.2. Data bus

Z606 and Z609, unidirectional buffers, isolates the A/D converter data bus from acquisition ram data bus.

Z101,Z201,Z104 and Z204 (Glitch capture board), unidirectional buffers, isolates the MINMAX1 and MINMAX2 bus from acquisition ram data bus. (OX8627 only)

Z607 and Z608, bidirectional buffers, connects the system processor data bus to acquisition ram data bus.

1.4.3.2.3. Control signals

The _OE and _W pins are connected to the system processor signals control throughout the time base controller.

The chip select pins are connected to the system address decode circuit Z201 via Z602.

1.4.4. Front panel offset acquisition

Active in digital mode, when the acquisition is stopped.
Used to control the vertical position of the displayed data waveform.
The inputs coupling are set to ground.
The outputs of the front panel vertical position potentiometers are applied to the A/D converters.The real time acquisition mode is used.
The vertical position controls range are about ±12 divisions (3 screens).
The A/D converters inputs range are about ±4 divisions (1 screen).
Three SEL_CADR control lines of analog multiplexer Z706 selects which of both front panel potentiometers is read .
The attenuator Z707 reduces the input signal level to set it back the dynamic range of the A/D converters.

1.4.4.1. Acquisition run

SEL_CADR0 = L SEL_CADR1 = L SEL_CADR2 = L

1.4.4.2. Acquisition stopped

1.4.4.2.1. CH1 vertical position acquisition

SEL_CADR0 = H SEL_CADR1 = H SEL_CADR2 = L

1.4.4.2.2. CH2 vertical position acquisition

SEL_CADR0 = H SEL_CADR1 = H SEL_CADR2 = H

1.5. DISPLAY CONTROLLER Z801 - sheet 8/19 - See ANNEX 2

Vertical resolution : 8 bits, 25 points per division

Horizontal resolution : 10 bits,100 points per division

The display system consists in the display controller, the display memory (Z802), and the X (Z804) and Y (Z803) DACs.
The display generates also a blanking signal.Output EFFAC pin 66.
The multiplexer Z808 is used to reduce the readout characters height.
Display state-machine clocks are generated by the time base controller 1 and 2MHz clock signals.

Display cycle

- If necessary, the system processor makes a display change.(Waveform data or readout characters update)
- The system processor programs the display controller to display a waveform data, a readout or a cursor.
- Datas are read from the memory and transfered to the ADCs.
- An interrupt to the system processor is generated (Output RST5.5visu goes high) by the display controller at the end of the display.

Cf. :
Figure 15 : Waveform display
Figure 16 : Readout display
Figure 17 : Vertical cursor display
Figure 18 : Horizontal cursor display
Figure 19 : End of display interrupt
Figure 20 : Mains synchronizing

Figure 15 - WAVEFORM DISPLAY

X	INUMX Pin 4 Z 804
Y	I_NUM _ Y1 Pin 8 Z 803
EFFAC	EFFAC Pin 66 Z 801
	EFF_NUM_ Pin 4 Z 806

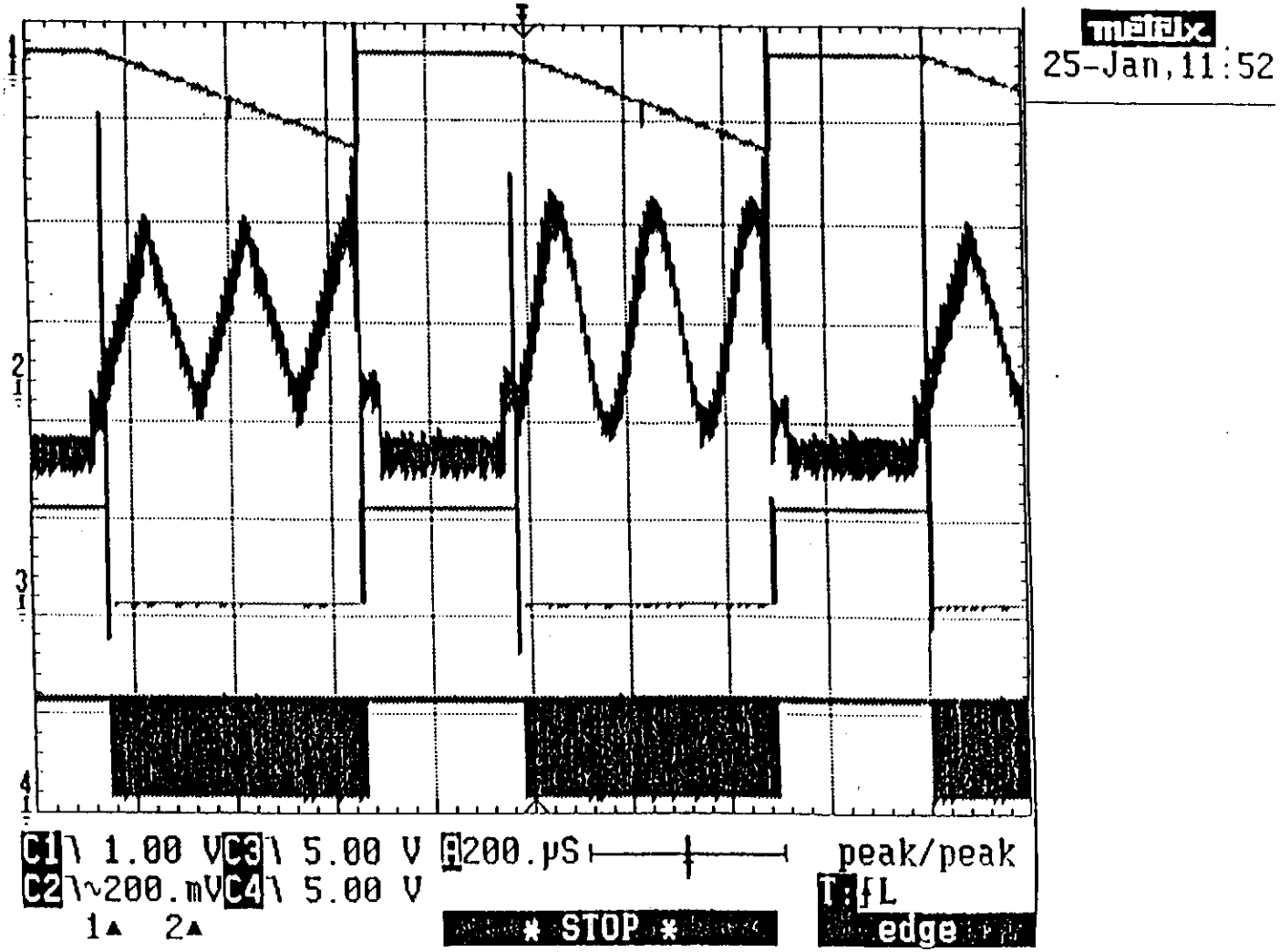


Figure 16 - READOUT DISPLAY

X I_NUM>

Pin 4 Z 804

Y I_NUM _Y1

Pin 8 Z 803

EFFAC EFF_NUM_

Pin 4 Z 806

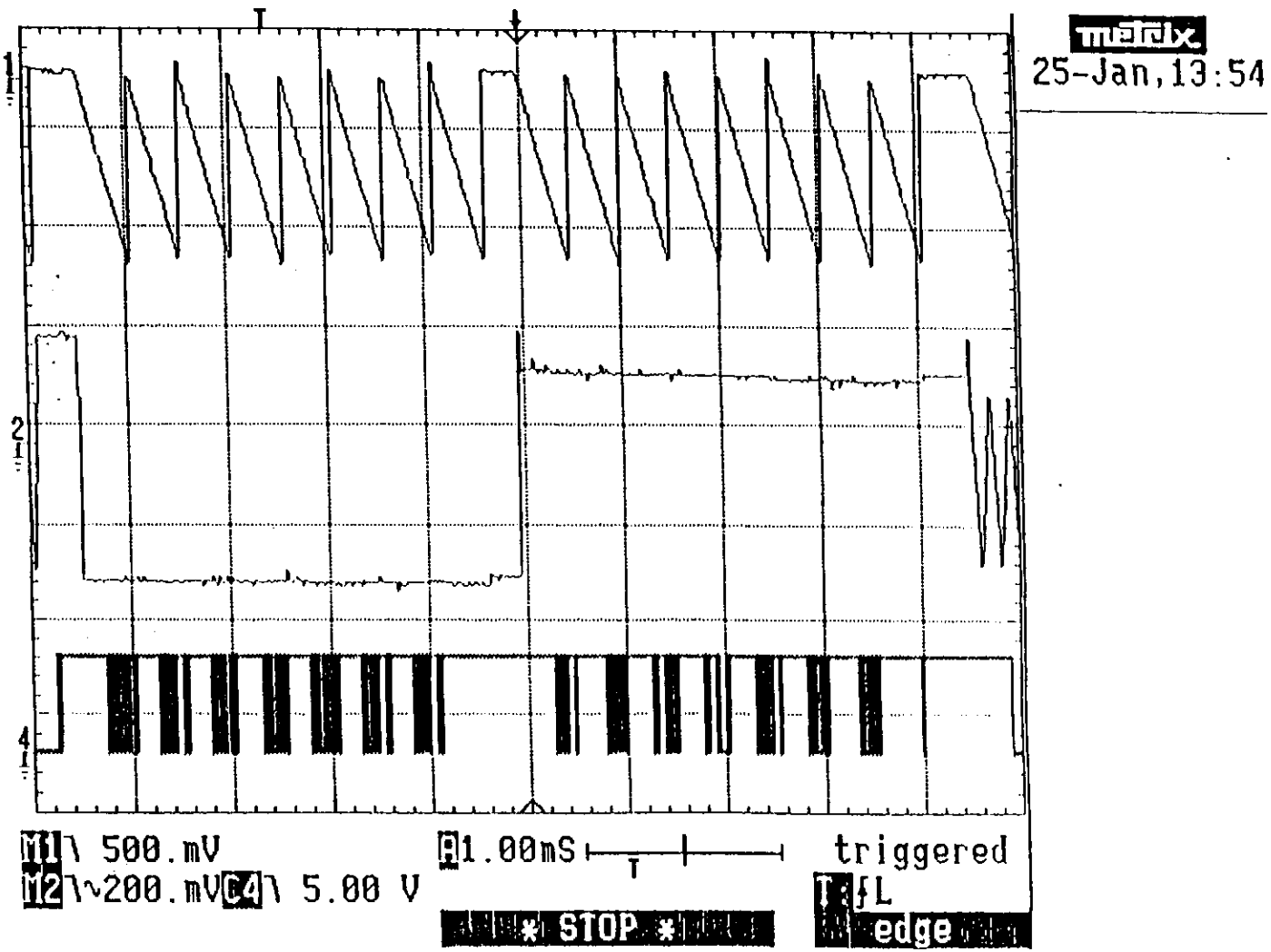


Figure 17 - VERTICAL CURSOR DISPLAY

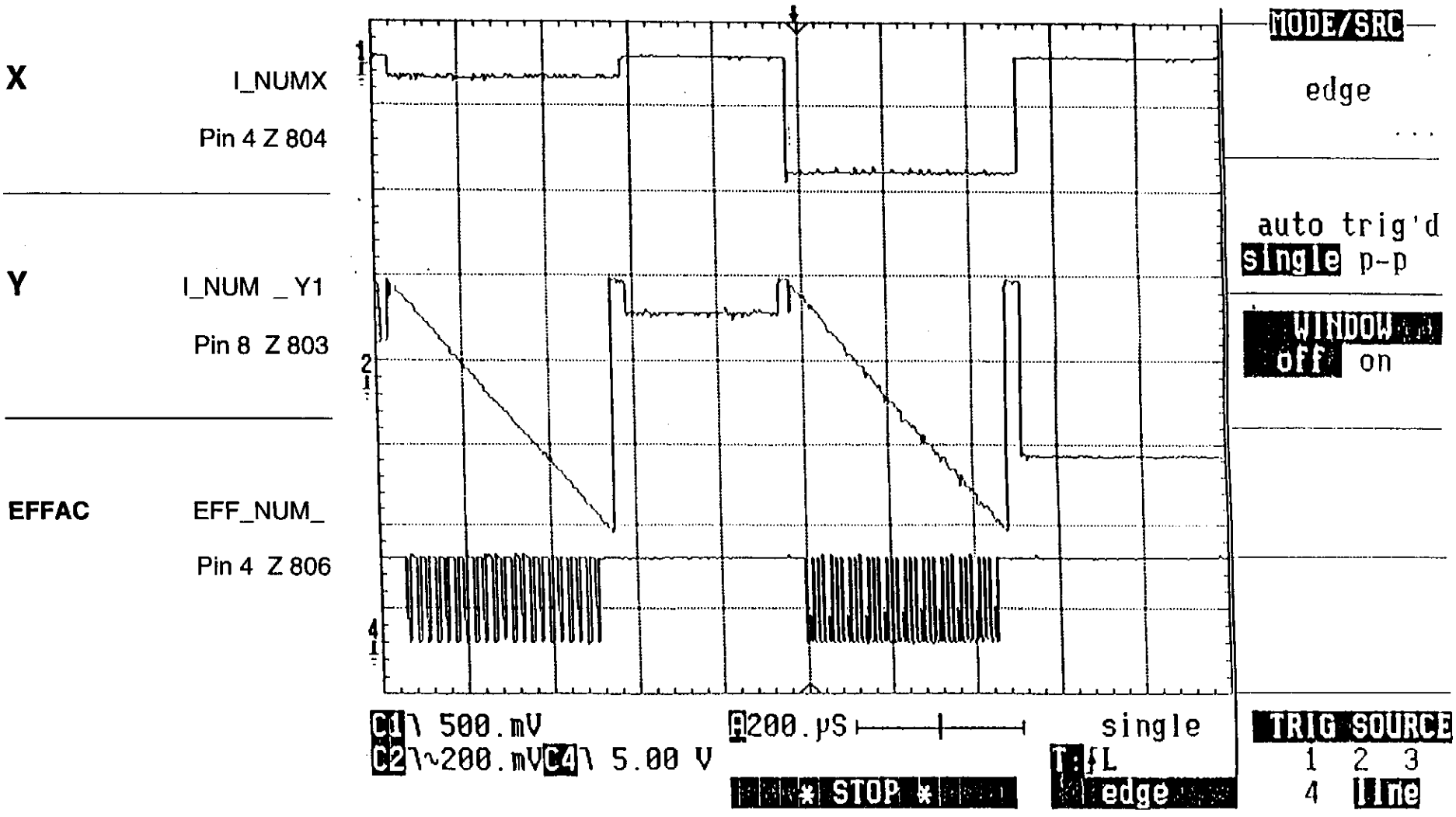


Figure 18 - HORIZONTAL CURSOR DISPLAY

X I_NUM>

Pin 4 Z 804

Y I_NUM _ Y1

Pin 8 Z 803

EFFAC EFF_NUM_

Pin 4 Z 806

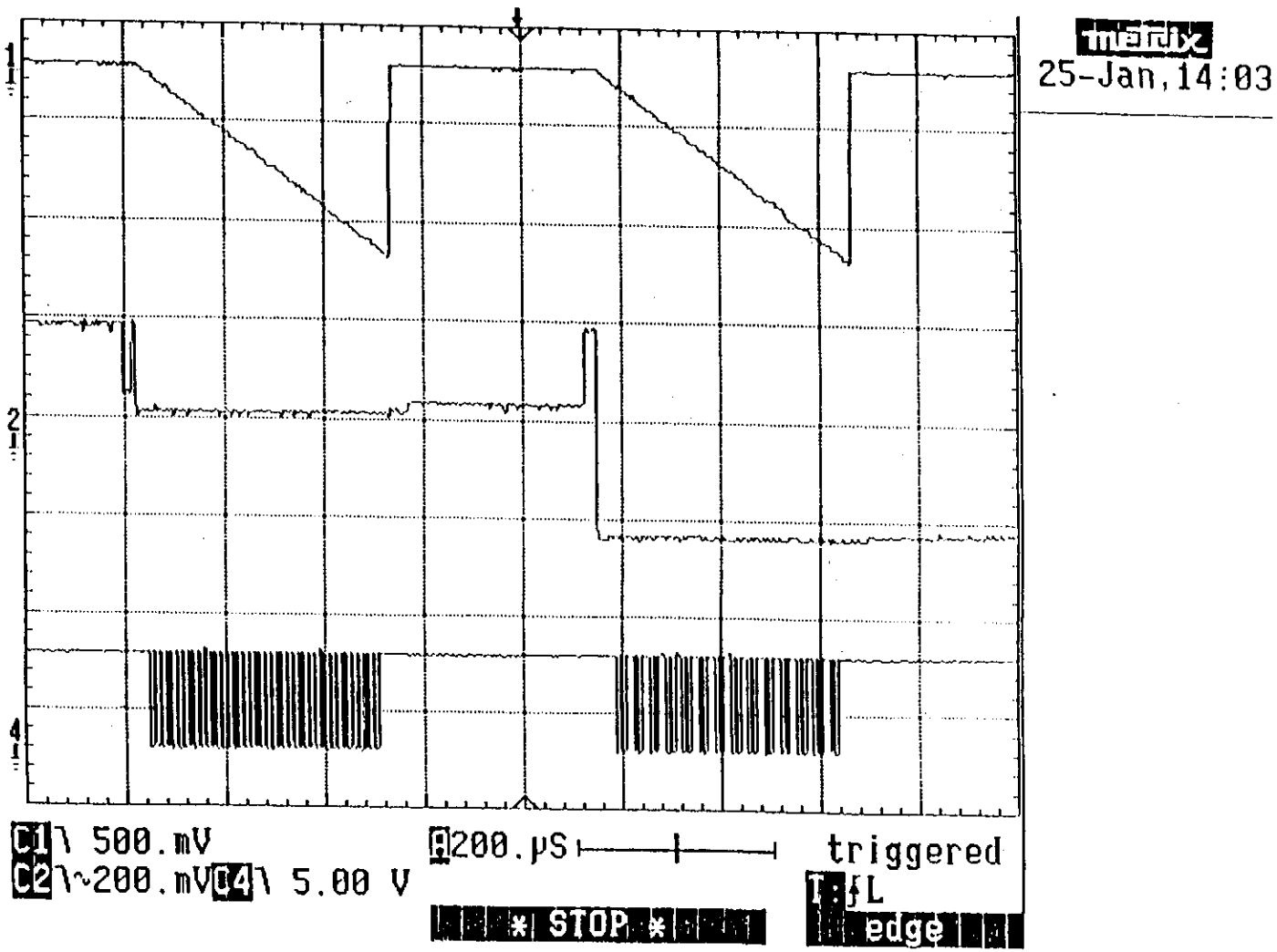


Figure 19 - END OF DISPLAY INTERRUPT

DISABLE -VISU

Pin 1 Z 611

RST5-5 VISU

Pin 10 Z 801

INT (1)

Pin 5 Z 614

SYNCHRO-SECTEUR

Pin 11 Z 806

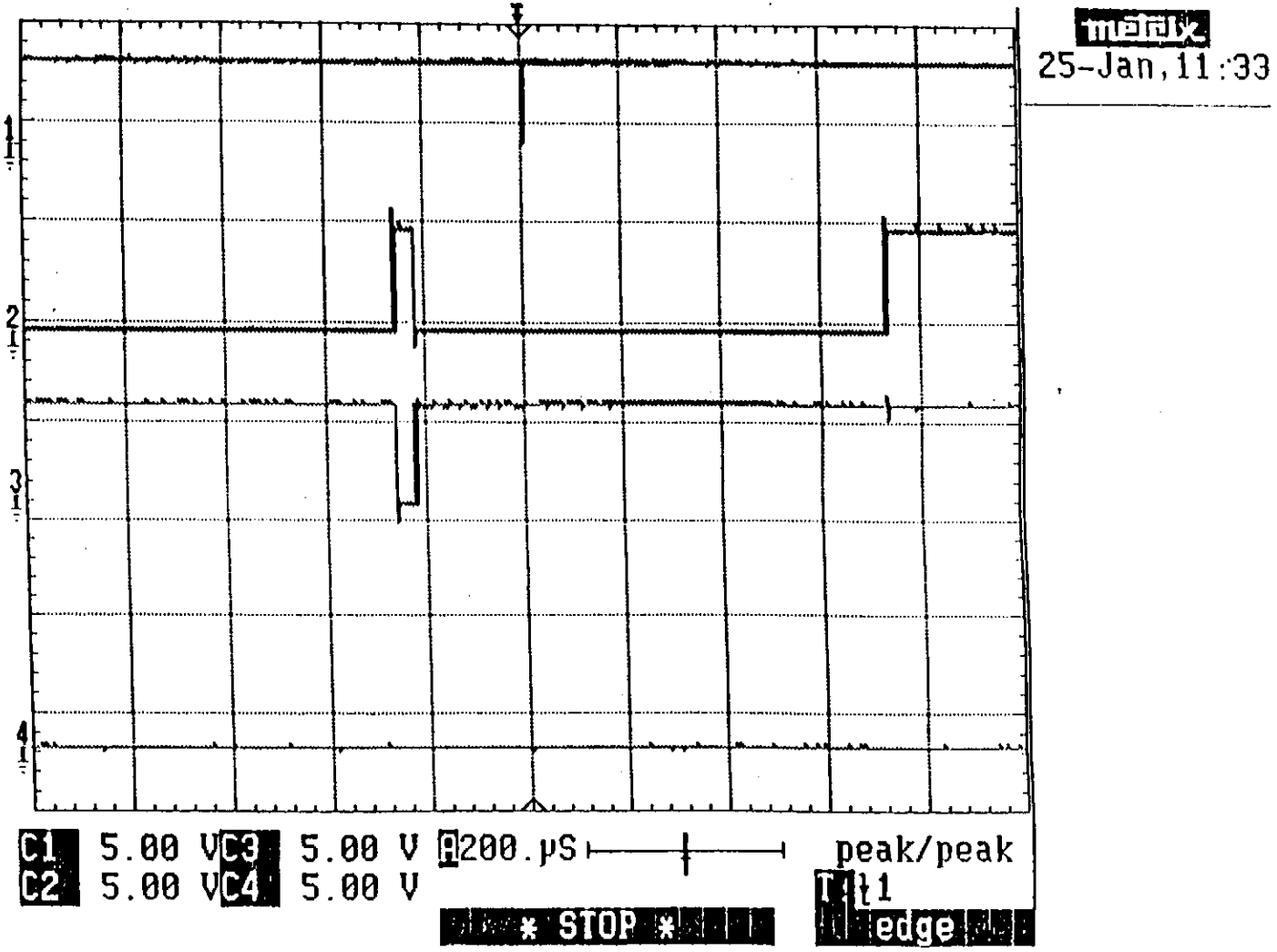


Figure 20 - MAINS SYNCHRONIZING

DISABLE -VISU

Pin 1 Z 611

RST5-5 VISU

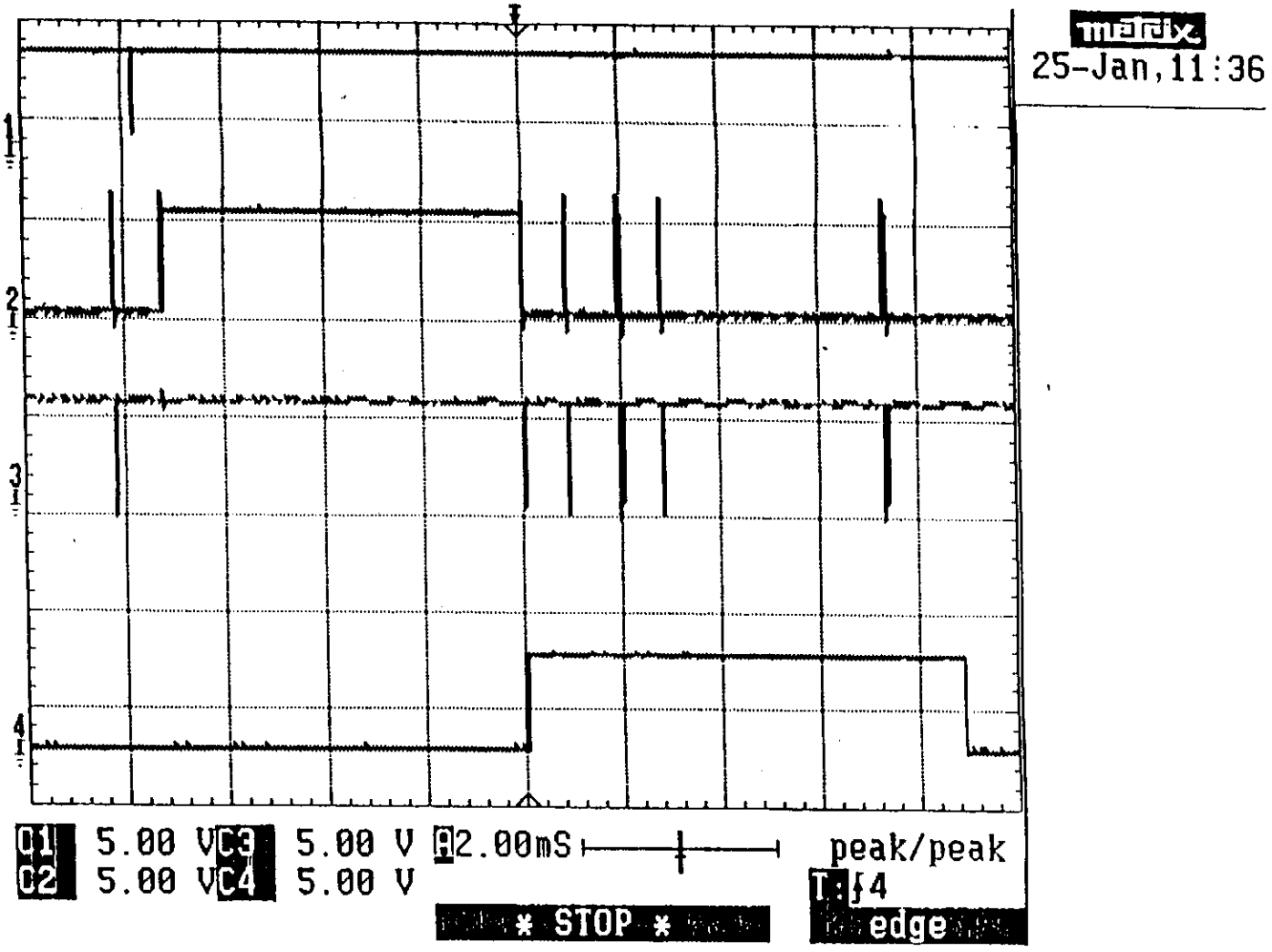
Pin 10 Z 801

INT (1)

Pin 5 Z 614

SYNCHRO-SECTEUR

Pin 11 Z 806



1.6 SYSTEM I/O

1.6.1. RS232 INTERFACE Z1001 sheet 10 - See Annex 3

The SCN68681 provides two independent full duplex asynchronous receiver/transmitter channels, a multi-function programmable 16 bit counter/timer, a multi-function 6 bit input port and a multi function 8 bit output port.
An external 3.6864 MHz quartz (Y1001) allows standard baud rates.

The first asynchronous communications port (TxDA and RxDA) provides the interfaces between the scope and external RS232 devices.
The output pin OP(0) is used as RTS control output signal.
The input pin IP(0) is used as CTS control input signal.
The CMOS levels input/output are level shifted (Z1002) to conform with the RS232 operating levels.

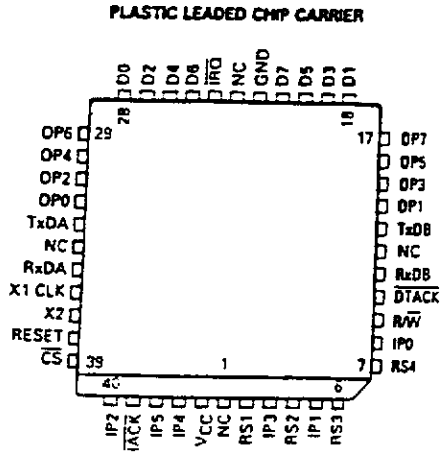
The second asynchronous communication port (TxDB and RxDB) is used to detect the presence of the calibration jumper.Refer to adjustment section.

Cf. : Figure 21 : 68681 pin assignments

1.6.2. GPIB INTERFACE - sheet 9/19 - See Annex 2

Only for the OX8627 oscilloscopes.
Z901 (NEC 7210) is a standard general purpose interface bus (GPIB) controller.
Z902 and Z903 are both lines drivers in accordance with IEEE488 standard.
The GPIB controller is driven by the time base controller 5MHz clock signal.

Figure 21 - 68681 pin assignments



1.7 TRIGGER LEVEL AND HORIZONTAL POSITION DIGITIZATION - SHEET 5/19

All the potentiometers of the front panel are not 'soft' controls.They directly activate a circuit function.The trigger level potentiometer is digitized for readout display.The horizontal position potentiometer is digitized at the beginning of the hardcopy.

The multiplexer Z503 select the pot to be read.The A/D converter (Z502) performs a 8 bit successive approximation.The A/D converter is driven by the time base controller 1MHz clock signal.

Cf. : Figure 22 : ADC bus timing. (Access with two wait states)

1.8. AUTO-SET- Sheet 11 /19 See Annex 2

OX8620 & OX8627 : The front panel processor performs this function.

1.9. POWER SUPPLY - Sheet 12/19

1.9.1. OX8620 & OX8627

The analog board switching power supply directly produces the 5VD and + 5VD_OPTION voltage.

Figure 22 - ADC BUS TIMING

CSEL - B (6)

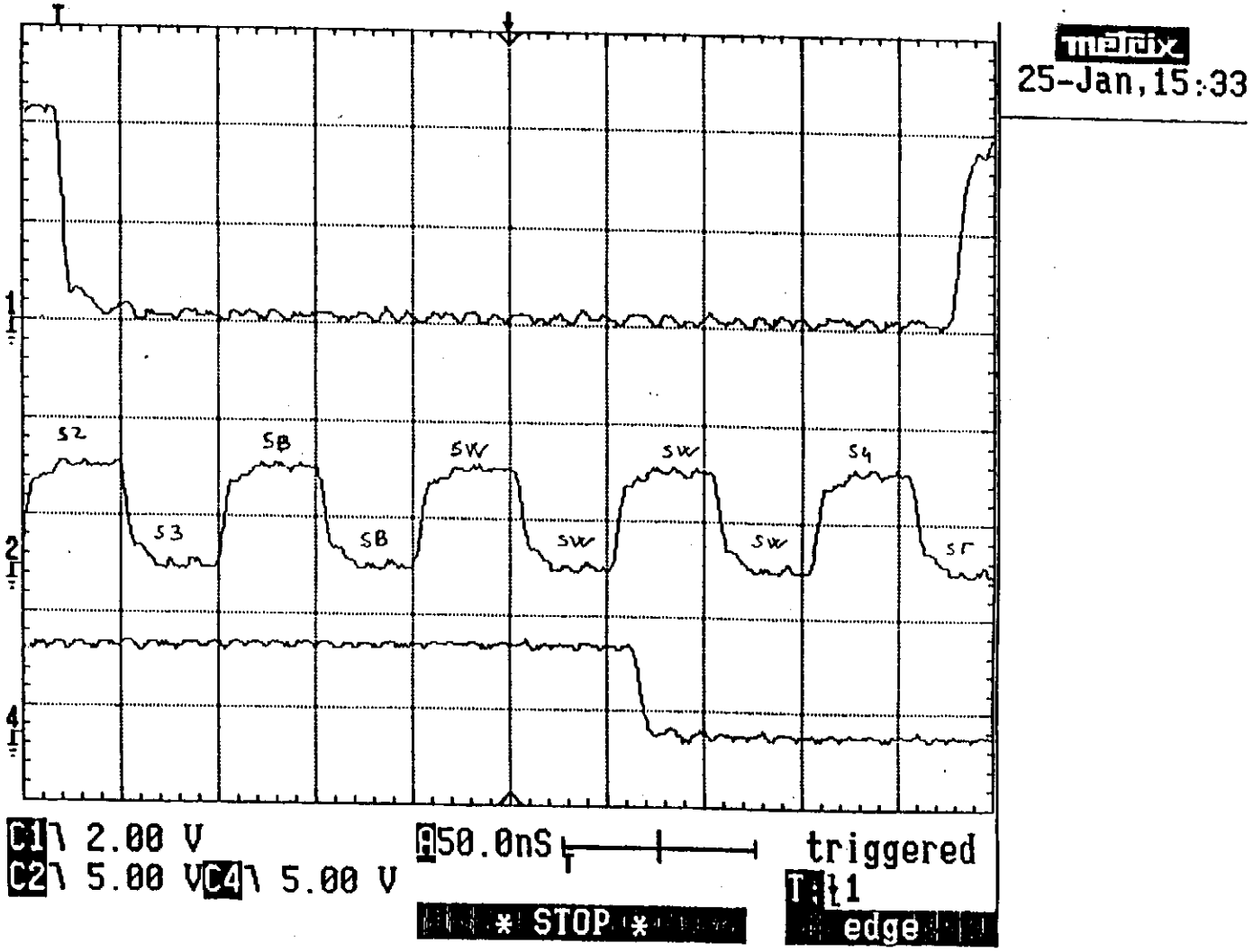
Pin 1 Z 502

CLKCPU

Pin 29 Z 101

DTACKN

Pin 24 Z 101



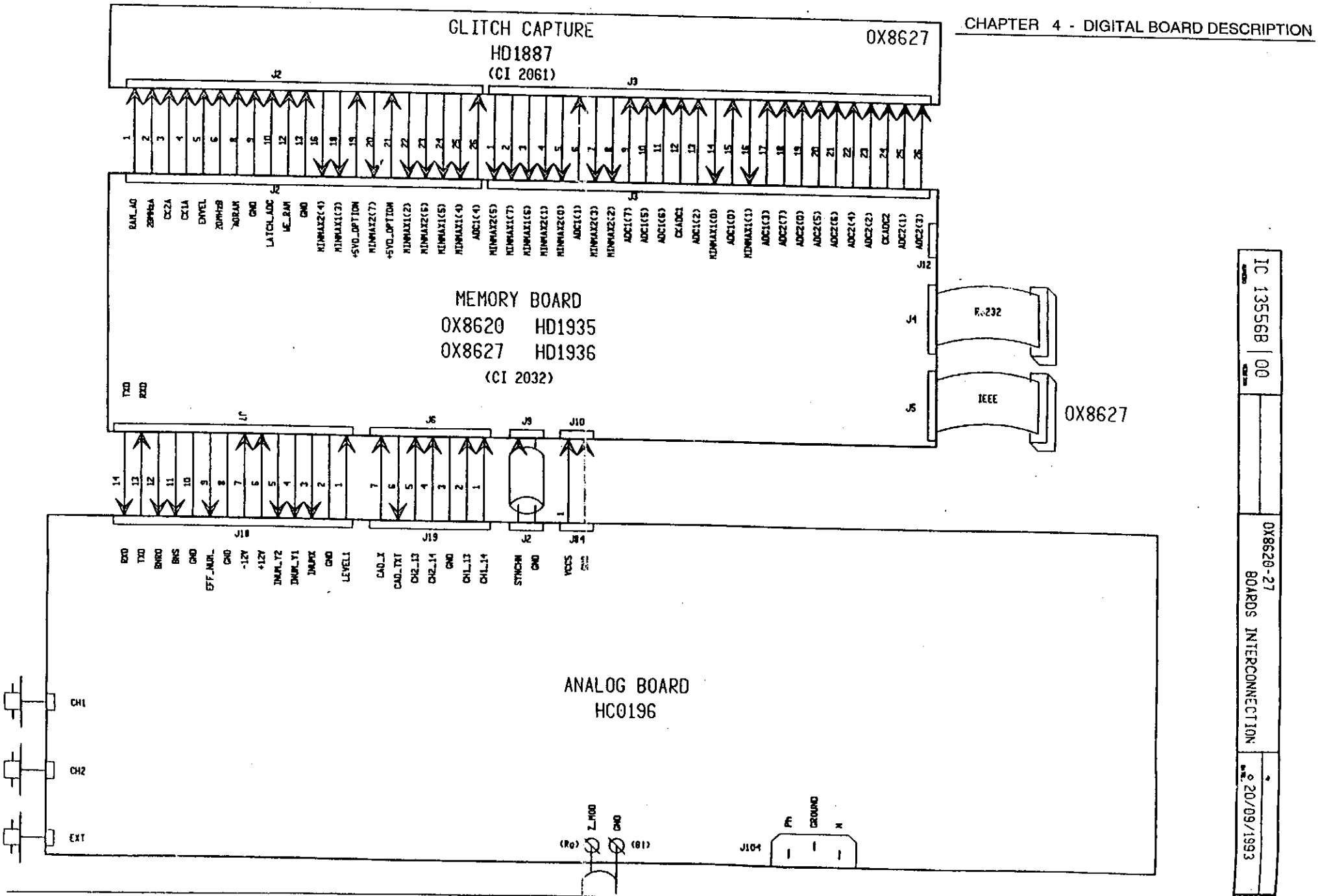
2. INTERCONNECT DIAGRAM

Cf. : Figure 23 : OX8020/27

3. PCB/PARTS LIST NUMBER

	PCB number	
Analog board	2086-05	2086-05
Digital board	2032-04	2032-04
Glitch capture board		2031-01
	OX8620	OX8627

	Parts list number	
Analog board	HC0196	HC0196
Digital board	HD1935	HD1936
Glitch capture board		HD1887
	OX8620	OX8627


GLITCH CAPTURE
HD1887
(CI 2061)
0X8627
J2
J3
MEMORY BOARD
0X8620 HD1935
0X8627 HD1936
(CI 2032)
J12
J4
RS-232
J5
IEEE
0X8627
J7
J6
J9
J10
J18
J19
J2
J11
ANALOG BOARD
HC0196
CH1
CH2
EXT
Z_MOD
GND
(R0)
(81)
J104
GROUND
IC 1355B | 00
0X8620-27
BOARDS INTERCONNECTION
20/09/1993

CHAPTER 5 - DIGITAL BOARD ADJUSTMENT

1. GETTING STARTED

The analog part of the oscilloscope must be adjusted and calibrated.
If necessary , refer to CHAPTER 3 - ANALOG BOARD ADJUSTMENT
The digital part of the instrument must be adjusted after a half an hour warm-up period.

2. CALIBRATION INSTRUMENTS TO BE USED

An oscilloscope calibrator
Square-wave signal (1KHZ/0.6V_{pp}).
A BF generator
Sine-wave or triangular-wave signal (50 KHz/0.8V_{pp}).

3. USEFUL DOCUMENTS

Marking layout of the analog board traditional components
CI 2086-05.
Marking layout of the digital board traditional components
CI 2032-04.

4. ADJUSTMENT STARTING

Switch off the instrument.
Remove the upper box.
Short-circuit $J11_1$ and $J11_4$
The J11 connector is located on the digital board.
Switch on the instrument.
The oscilloscope screen displays :

Etalonnage memoire OX862x **Lancer**

Press the HARDCOPY key to launch the adjustment.

5. RUNNING

When adjusting, the keys and the knobes of the front panel are disabled.
For each step of the calibration :
The necessary operating mode is automatically configurated.
The operator must adjust as requested and valid by pressing HARDCOPY.

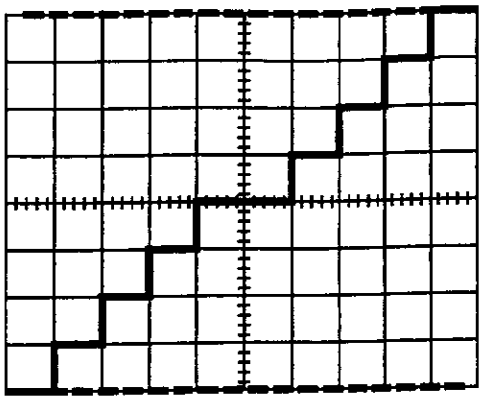
It is impossible to set back to previous step.
If necessary, switch off the instrument and re-start the procedure.
The calibration process consists in :
9 hard adjustments.(Action on adjustable resistors)
4 soft adjustments.(Digitization of the front panel potentiometers)

5.1 VERTICAL GAIN AND OFFSET ADJUSTEMENT

The screen displays :

GAIN Y REST. OFFSET REST. Quit

Action :
Adjust R637 (gain) and R643 (offset) to align the cursors on the first and the last horizontal graticule line.



Adjustment positions :
R637 : Main board
R643 : Main board
Valid this adjustment by pressing the HARDCOPY key.

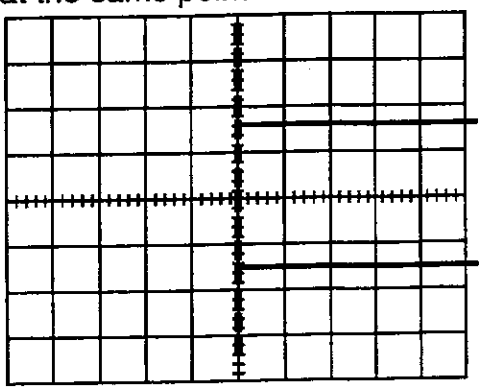
5.2 ANALOG/DIGITAL X POSITION CONCORDANCE

5.2.1 Offset adjustment

The screen displays :

Depart de trace au centre.CENTR X TRACE Quit

Action :
Set the trace starting point on the mid-vertical line with the horizontal position button of the front panel.
Position the left cursor at the same point with R1418.



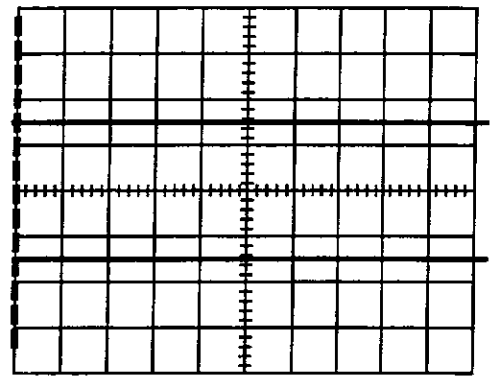
Adjustment position :
R1418 : Main board
Valid this adjustment by pressing the HARDCOPY key.

5.2.2 Gain adjustment

The screen displays :

Depart de trace a gauche.GAIN X NUM Quit

Action :
Set the trace starting point on the first vertical line with the horizontal X position button of the front panel.
Position the left cursor at the same point with R1430.
When sweeping the left half of the screen, check that both cursor and starting point stay together.



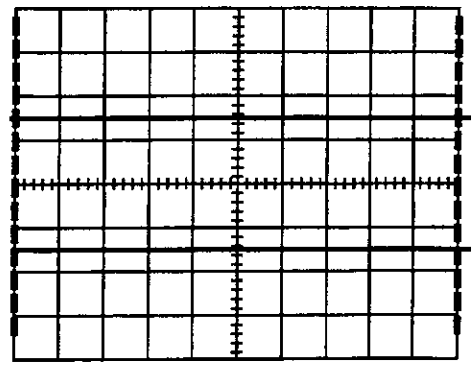
Adjustment position :
R1430 : Main board
Valid the adjustment by pressing the HARDCOPY key.

5.3 HORIZONTAL GAIN ADJUSTMENT

The screen displays :

GAIN X NUM. R811 carte memoire. Quit

Action :
Set the starting point of the trace on the first vertical line with the horizontal position button of the front panel.
Adjust R811 to position the right cursor on the last vertical line, at the right of the screen.



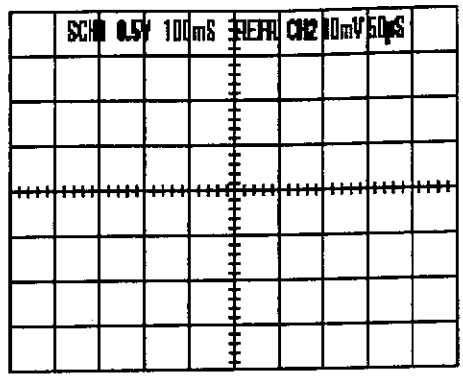
Adjustment position :
R811 : Digital board
Valid the adjustment by pressing the HARDCOPY key.

5.4 TEXT CENTRING

The screen displays :

Centrage Texte: CENTR X READ-OUT Quit

Action :
Use the front panel keys '<-' and '->' to centre the upper line of the text.



Valid the adjustment by pressing the HARDCOPY key.

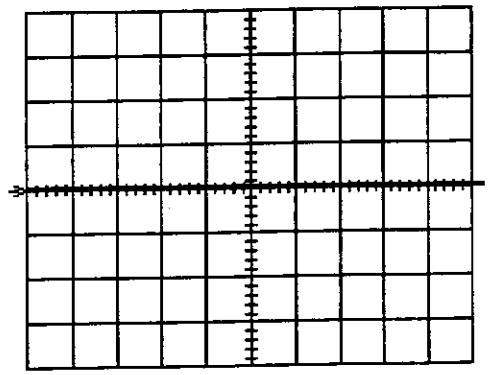
5.5 ACQUISITION CH1

5.5.1 CH1 front panel offset cancelation

The screen dispalys :

Centrer trace CH1 en Y Quit

Action :
Set the trace on the horizontal mid-line of the screen with the vertical position CH1 button of the front panel.



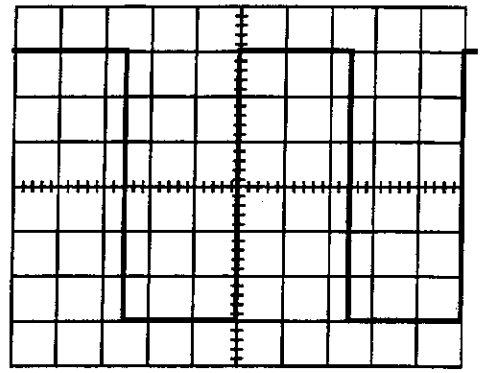
Valid the adjustment by pressing the HARDCOPY key.

5.5.2 CH1 acquisition gain and offset

The screen displays :

Carre 1 KHz 0.6Vpp/CH1: GAIN1 OFFS1 Quit

Action :
Set the trace on the horizontal mid-line of the screen with R711. **Do not use the button of the front panel.**
Inject on CH1, a 1KHz, 0.6V_{pp} square-wave signal.
Adjust R707 for a 6 division display.



Adjustment position :
R711 : Digital board
R707 : Digital board
Valid the adjustment by pressing the HARDCOPY key.

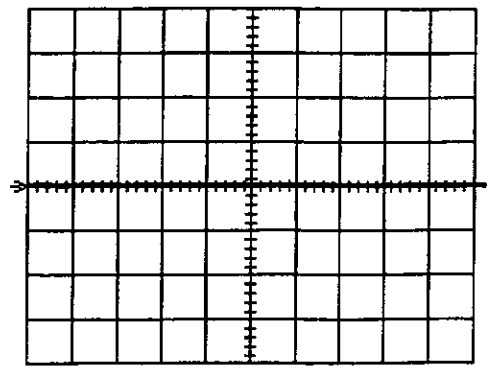
5.6 CH2 ACQUISITION

5.6.1 CH2 front panel offset cancelation

The screen displays :

Centrer trace CH2 en Y Quit

Action :
Set the trace on the horizontal mid-line of the screen with the vertical position CH2 button of the front panel.



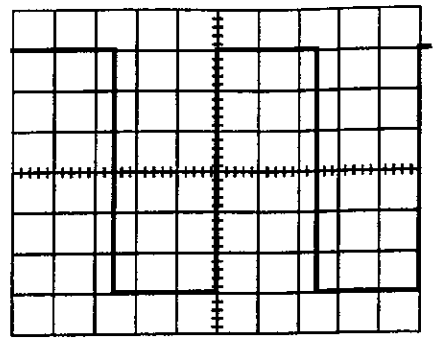
Valid the adjustment by pressing the HARDCOPY key.

5.6.2 CH2 acquisition gain and offset

The screen displays

Carre 1 KHz 0.6Vpp/CH2: GAIN2 OFFS2 Quit

Action :
Set the trace on the horizontal mid-line of the screen with R731.**Do not use the button of the front panel.**
Inject on CH2 a square-wave signal 1KHz ,0.6V_{pp}.
Adjust R728 for a 6 division display.



Adjustment position :
R731 : Digital board
R728 : Digital board
Valid the adjustment by pressing the HARDCOPY key.

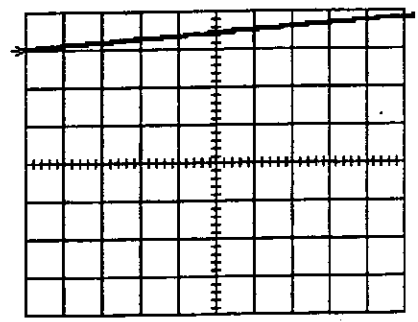
5.7 TRIGGER LEVEL BUTTON DIGITIZATION

5.7.1 +3 Div trigger level

The screen displays :

CH1: SIN 50Khz 0.8Vpp LEVEL sur +3 Div Quit

Action :
Inject a 50 KHz 0.8V_{pp} sine-wave signal on CH1 input.
Adjust the LEVEL button of the front panel to get the trace starting on the third horizontal line from the top of the screen (+3 Div). **Do not use the CH1 front panel position.**



Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

Lecture du niveau de declenchement

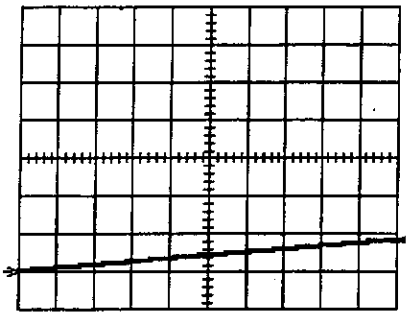
5.7.2 -3 Div Trigger level (Positive slope)

The screen displays :

CH1: SIN 50Khz 0.8Vpp LEVEL sur -3 Div Quit

Action :

Set the LEVEL button of the front panel to get the trace starting on the third horizontal line of the lower part of the screen (-3 Div). **Do not use the CH1 front panel vertical position.**



Valid the adjustment by pressing the HARDCOPY key.

The screen displays :

Lecture du niveau de declenchement

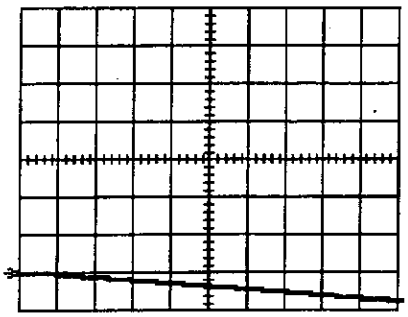
5.7.3 Positive/Negative slope offset

The screen displays :

Offset front negatif. LEVEL sur -3 Div Quit

Action :

Set the LEVEL button of the front panel to get the trace starting on the third horizontal line of the lower part of the screen (-3 Div). **Do not use the CH1 front panel vertical position.**



Valid the adjustment by pressing the HARDCOPY key.

The screen displays :

Lecture du niveau de declenchement

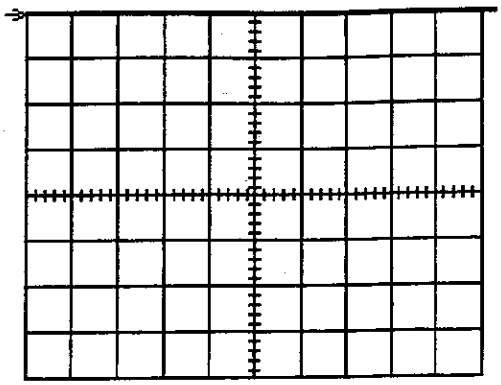
5.8 ANALOG/DIGITAL CH1 POSITION CONCORDANCE

5.8.1 +4 Div offset

The screen displays :

Trace CH1 sur +4 Divisions **Quit**

Action :
Set the trace on +4 Div with the CH1 position button of the front panel.



Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

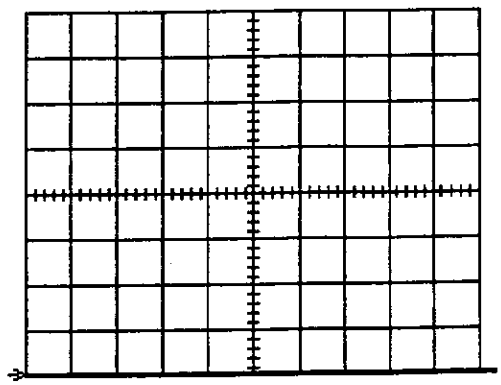
Lecture du decadrage

5.8.2 -4 Div offset

The screen displays :

Trace CH1 sur -4 Divisions **Quit**

Action :
Set the trace on -4 Div with the CH1 position button of the front panel.



Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

Lecture du decadrage

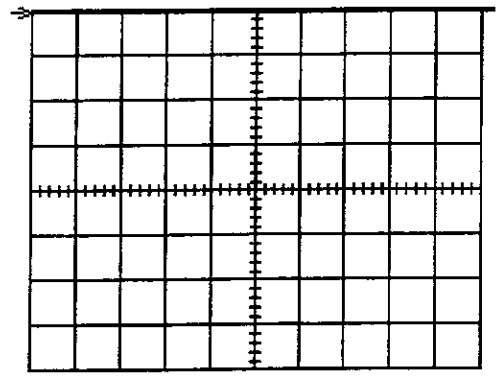
5.9 ANALOG/DIGITAL CH2 POSITION CONCORDANCE

5.9.1 +4 Div offset

The screen displays :

Trace CH2 sur +4 Divisions **Quit**

Action :
Set the trace on +4 Div with the CH2 position button of the front panel.

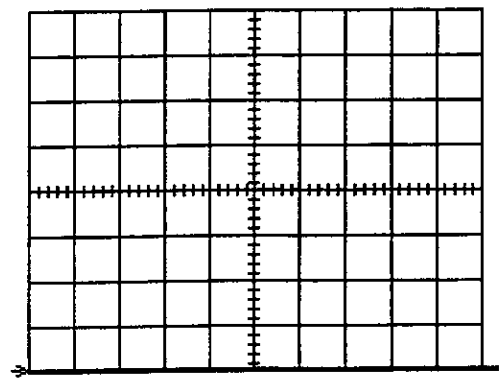


Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

Lecture du decadrage

5.9.2 -4 Div offset

The screen displays :
Trace CH2 sur -4 Divisions **Quit**
Action :
Set the trace on -4 Div with the CH2 position button of the front panel.



Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

Lecture du decadrage

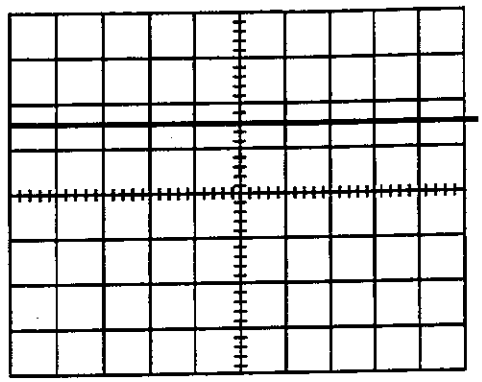
5.10 X POSITION BUTTON DIGITIZATION

5.10.1 Trace starting from the left hand side of the screen

The screen displays :

Trace CH1 calee sur bord gauche **Quit**

Action :
Set the trace start on the first vertical line of the screen with the X position button of the front panel.



Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

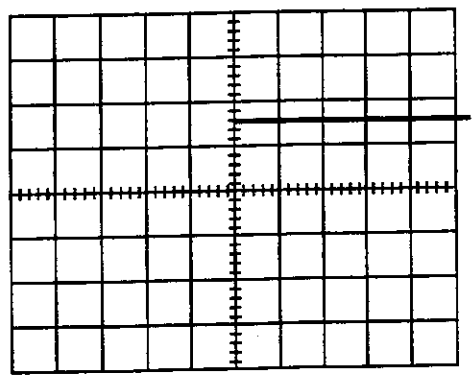
Lecture de la position horizontale

5.10.2 Trace starting in the center

The screen displays :

Trace CH1 calee sur axe Y central **Quit**

Action :
Set the trace start on the vertical mid-line with the X position button of the front panel.



Valid the adjustment by pressing the HARDCOPY key.
The screen displays :

Lecture de la position horizontale

5.11 END OF ADJUSTMENT

Save the 'soft' adjustments in the EEPROM of the front panel

The instrument is adjusted..

The screen displays :

OX862x Etalonne **Quit**

Quit the adjustment program by pressing the HARDCOPY key.

ANNEXES

- ❑ **Annex 1 - General synoptic and Front panel synoptic**...2 pages

- ❑ **Annex 2 - Schematic diagrams - CI 2086-05.1** .....19 p.
  + Components location .....2 p.
  Schematic diagrams - CI 2086-08 .....19 p.
  + Components location .....2 p.
  List of modifications.....1 p.

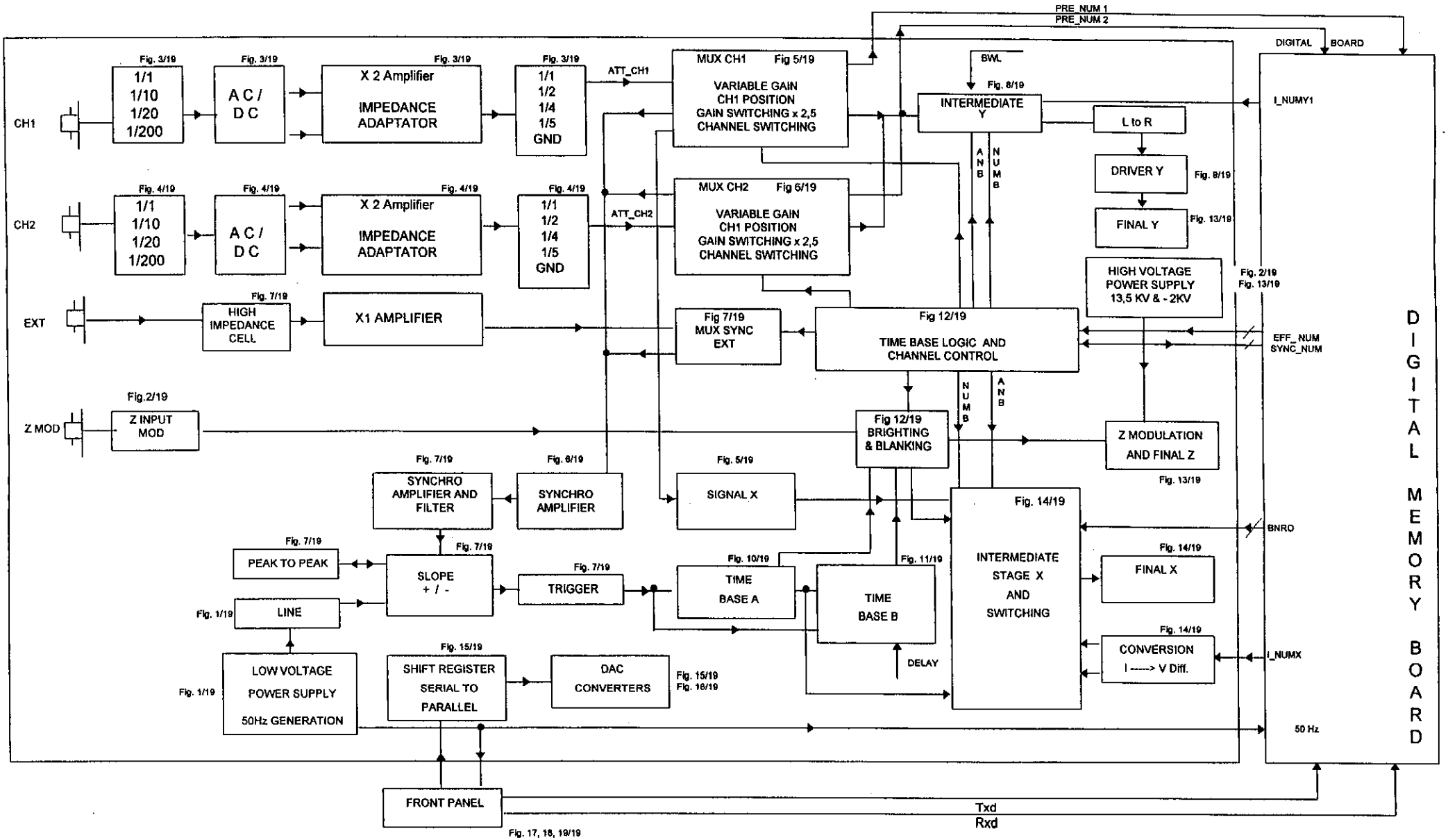
- ❑ **Annex 3 - CI 2032-4 - Components location**.....2 p.
  Digital board schematics
  OX 8620 ---> HD 1935
  OX 8627 ---> HD 1936 .....13 p.
  ---> HD 1887 Glitch capture .....2 p.

- ❑ **Annex 4 - Modifications** .....5 p.

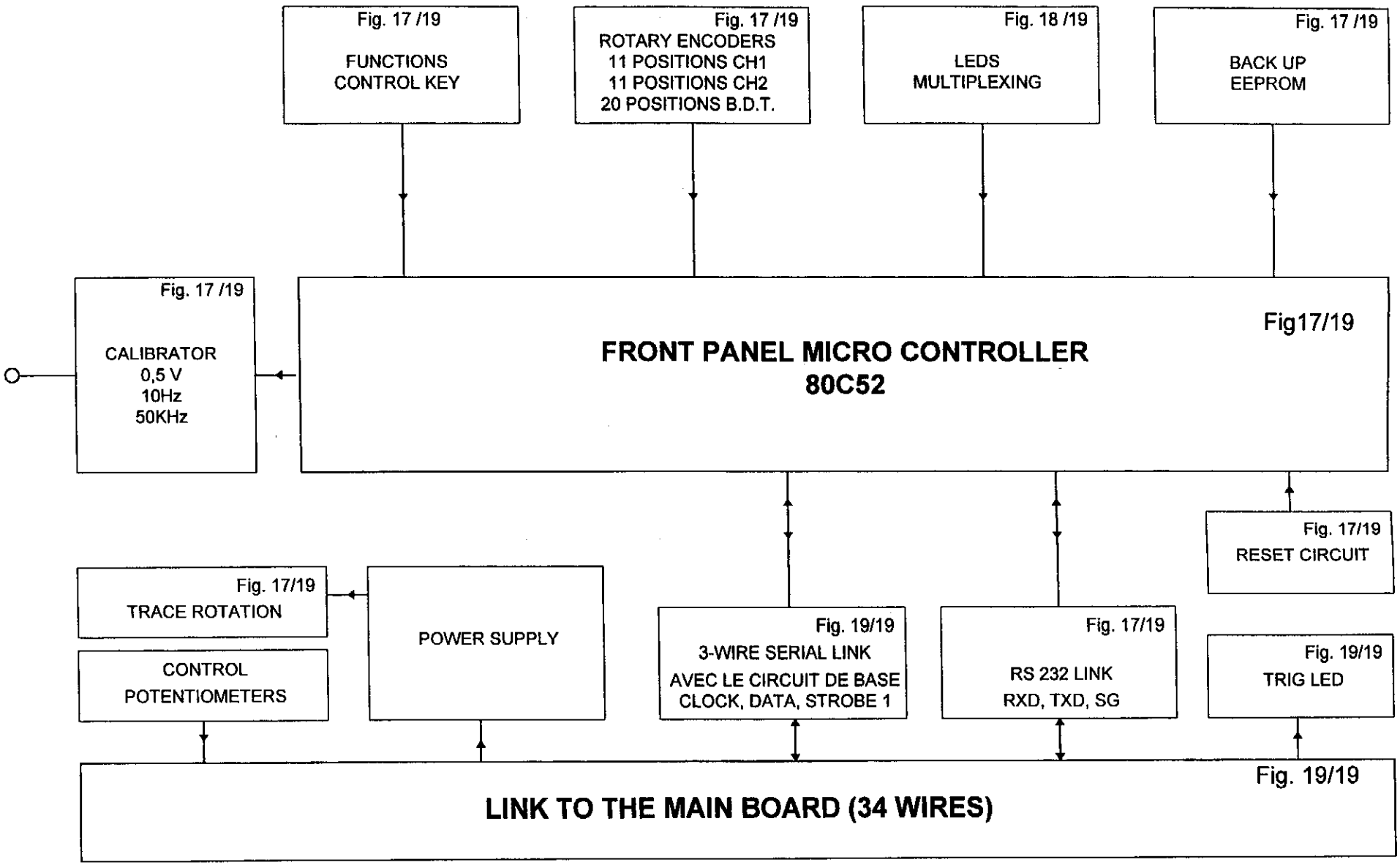
- ❑ **Annex 5 - Parts list**.....7 p.

ANNEX 1 - GENERAL SYNOPTIC & FRONT PANEL SYNOPTIC

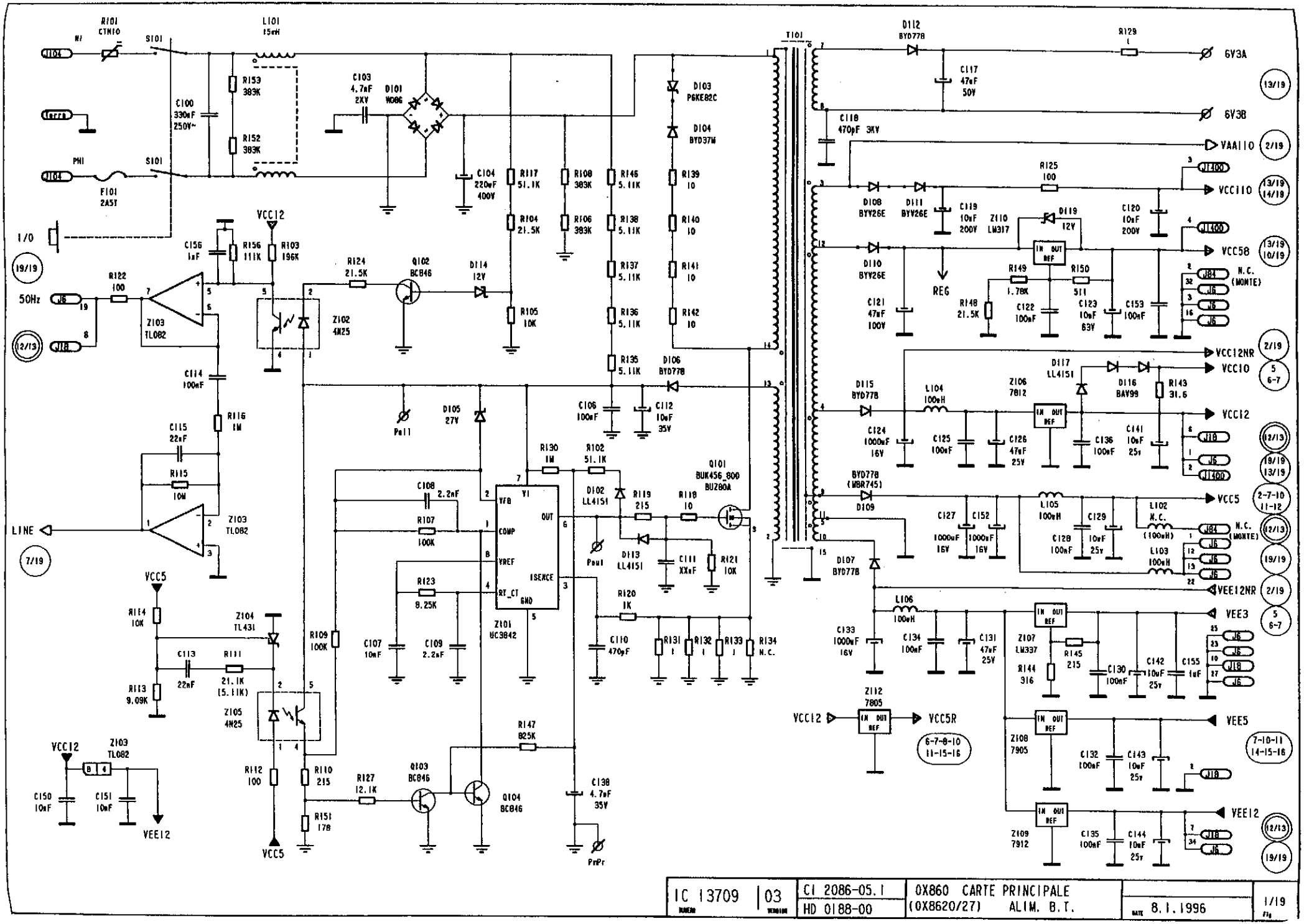
GENERAL SYNOPTIC (CI 2080) OX 8620 / OX 8627 AND ITS PERIPHERALS



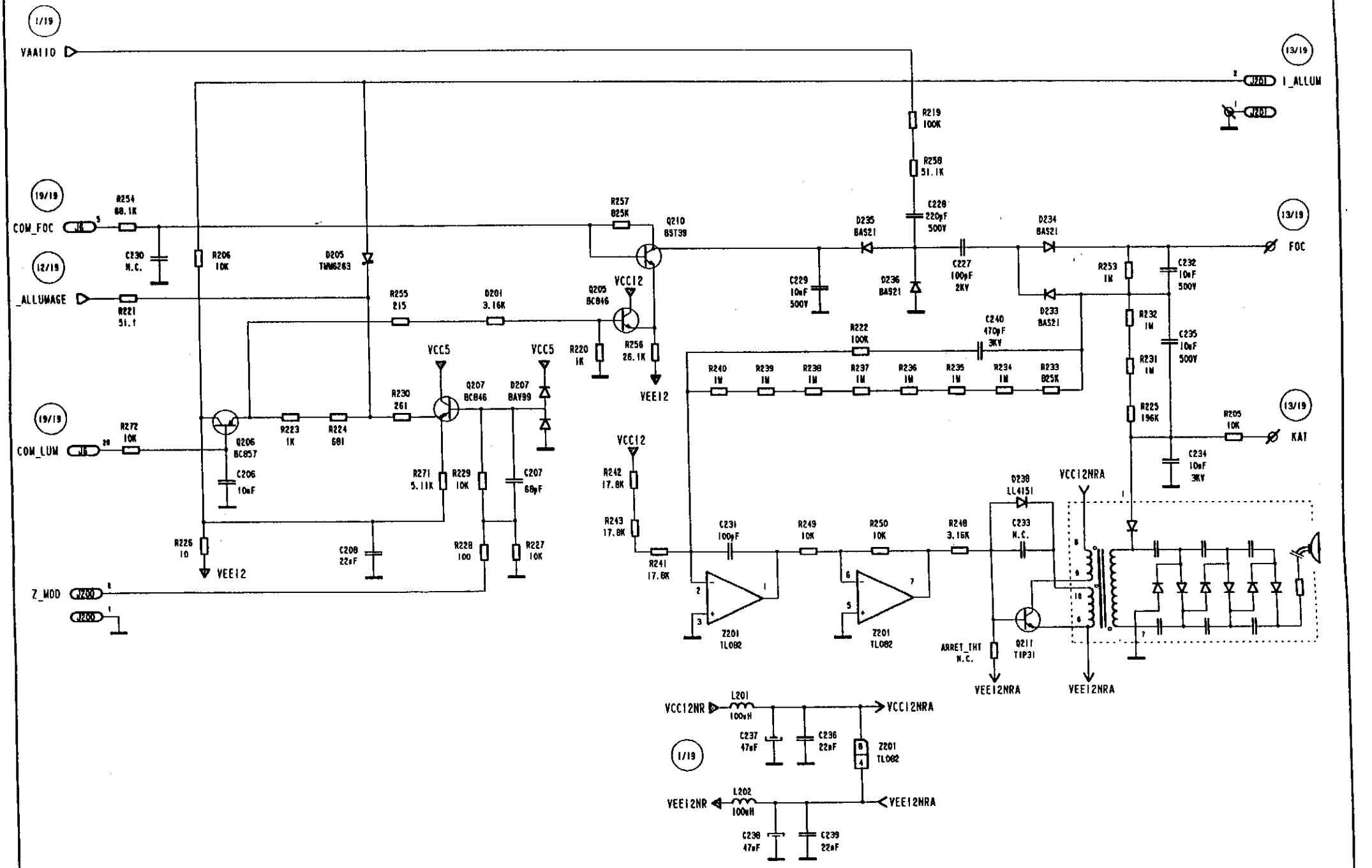
BLOCK DIAGRAM AND LAYOUT - FRONT PANEL



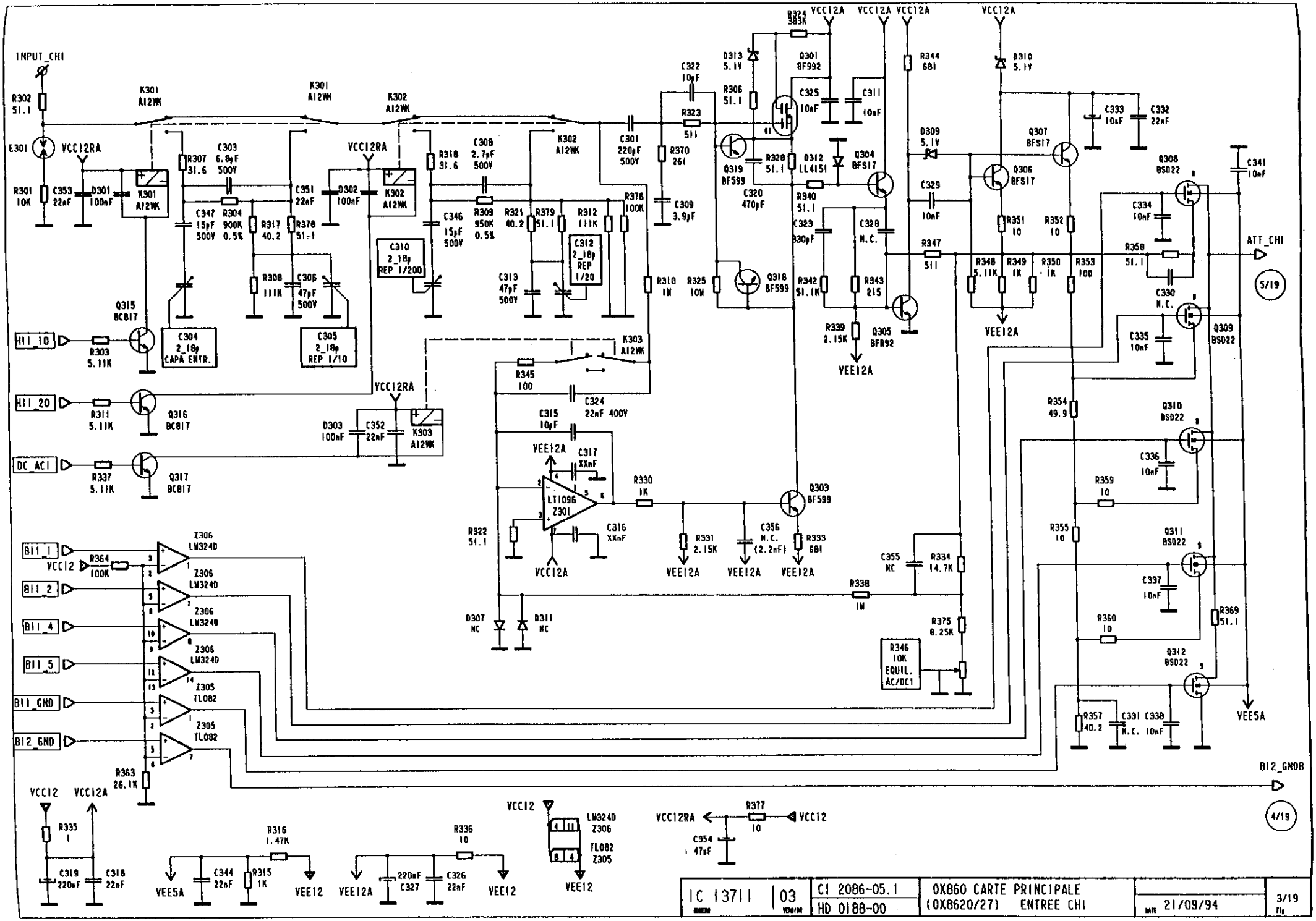
ANNEX 2 - SCHEMATICS - CI 2086-05.1 & COMPONENTS LOCATION

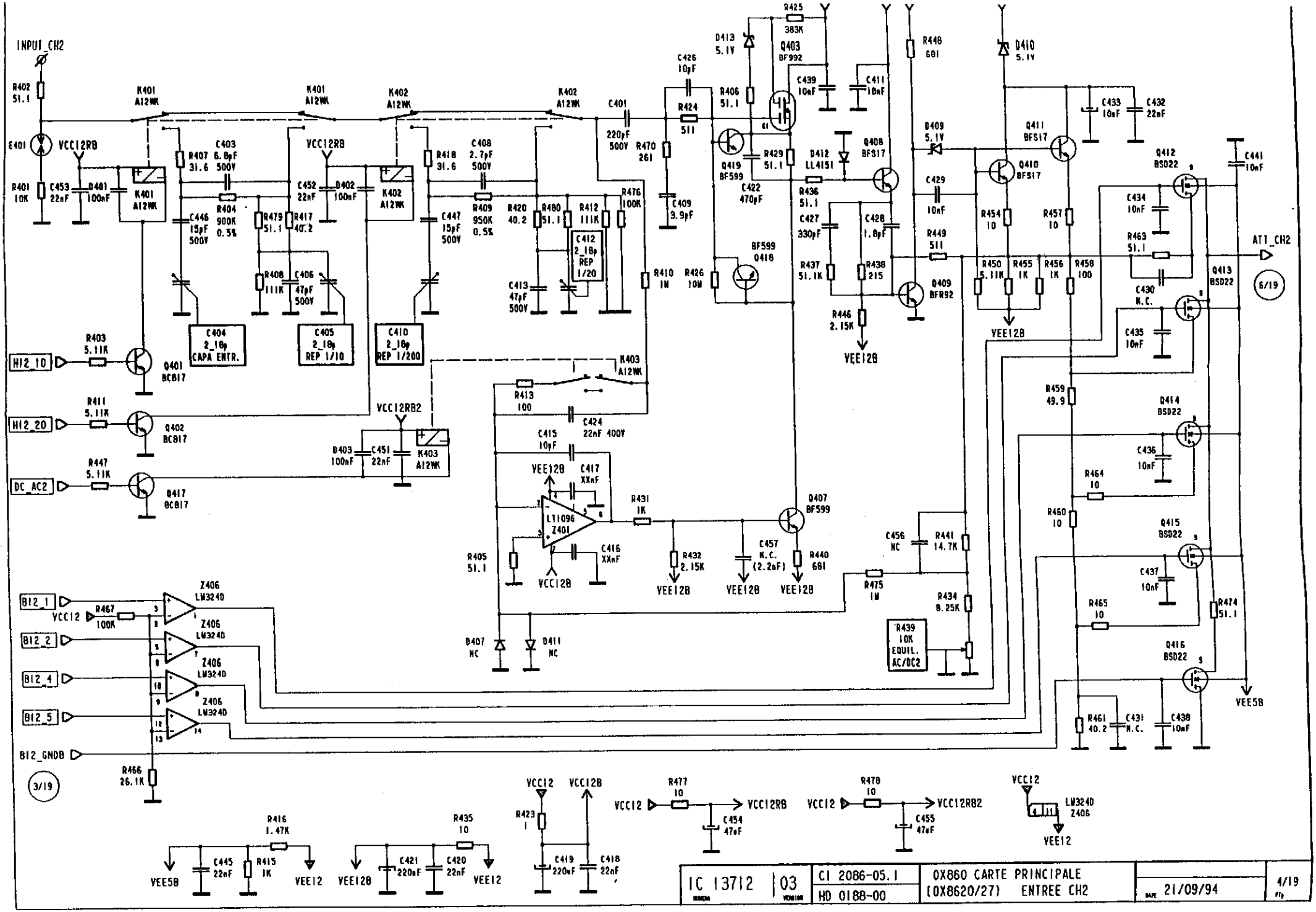


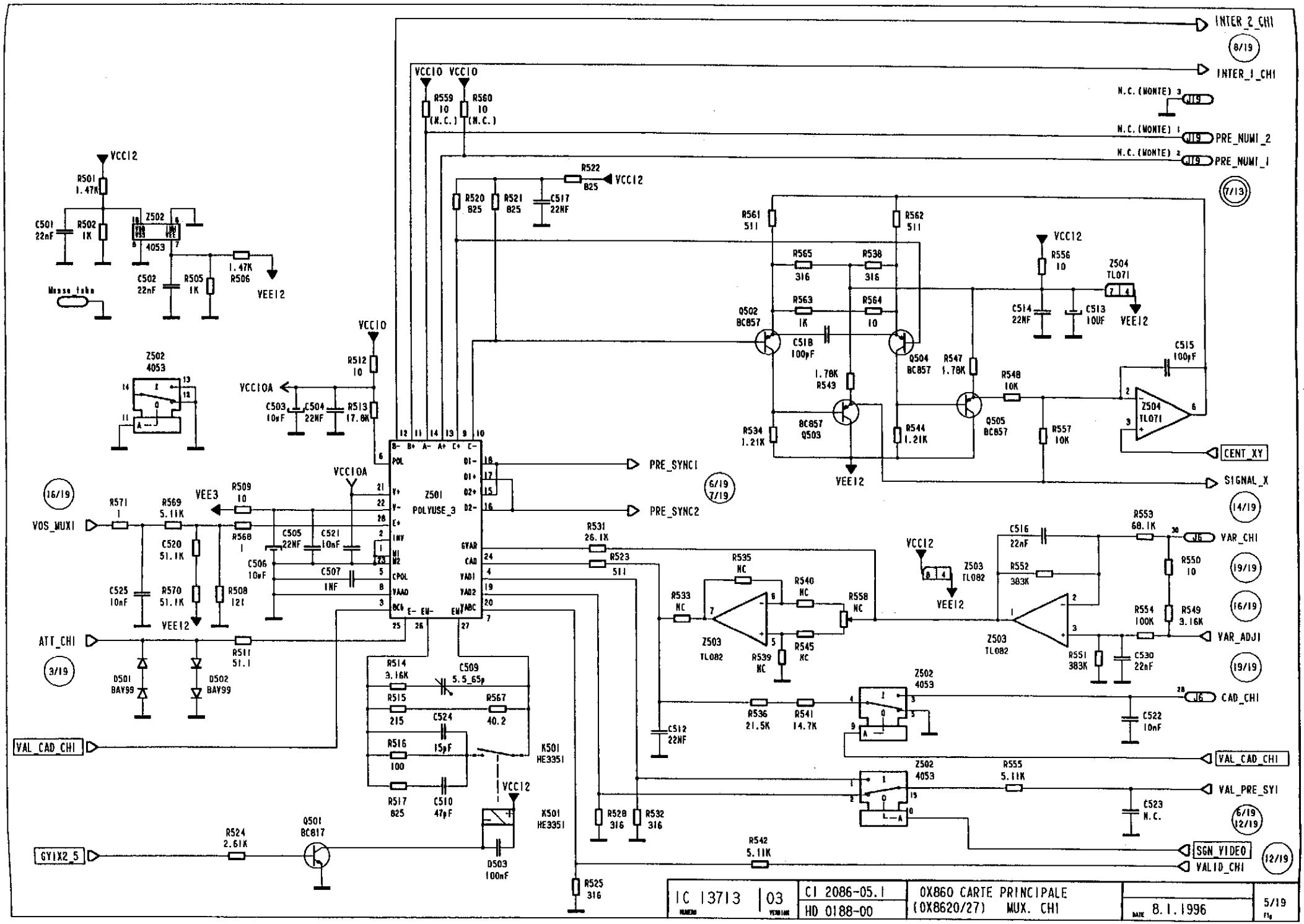
IC 13709	03	CI 2086-05.1	0X860 CARTE PRINCIPALE		1/19
		HD 0188-00	(0X8620/27) ALIM. B.T.	8.1.1996	



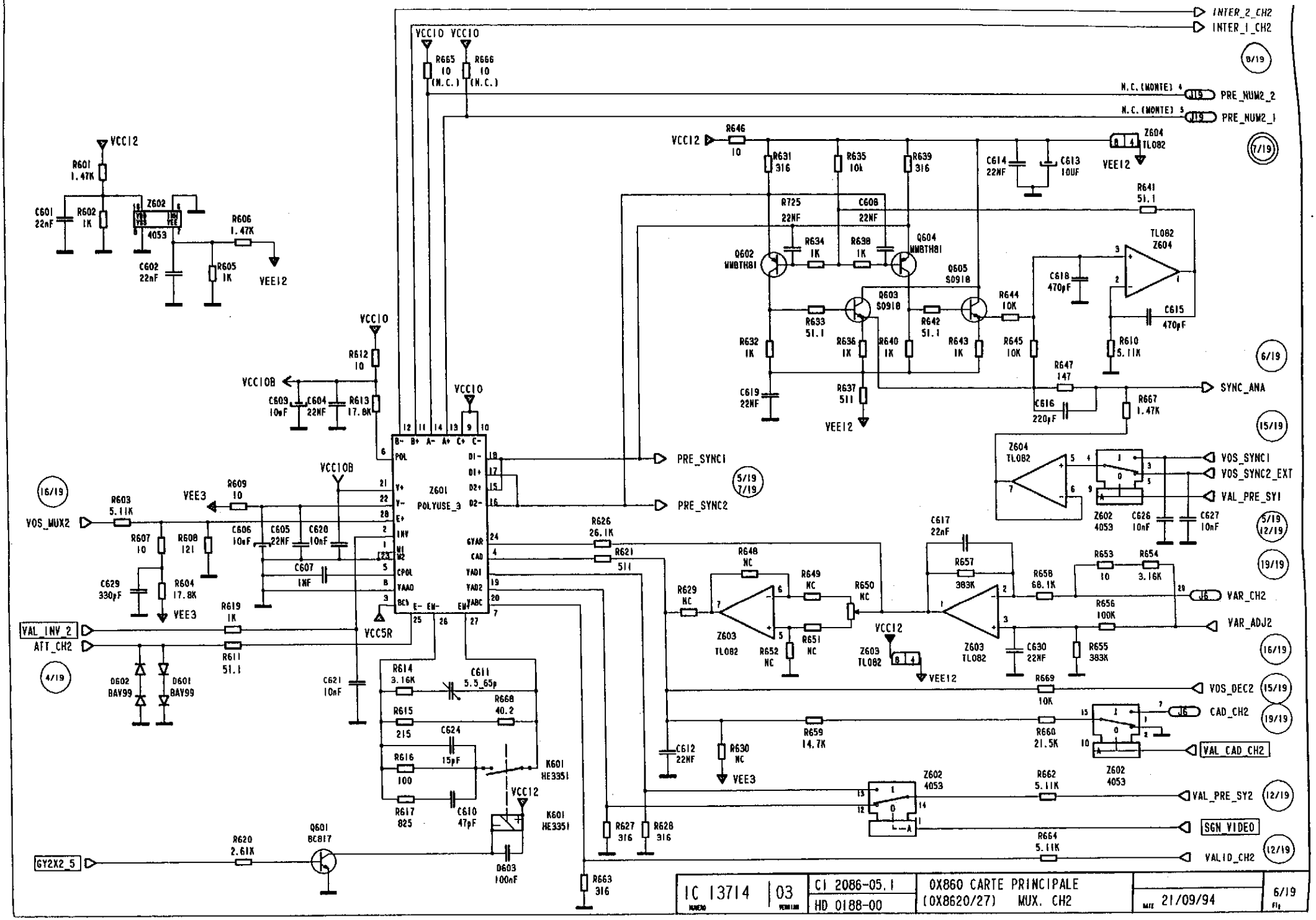
IC 13710	03	C1 2086-05.1	0X860 CARTE PRINCIPALE	DATE 8.1.1996	2/19
		HD 0188-00	(0X8620/27) T.H.T.		

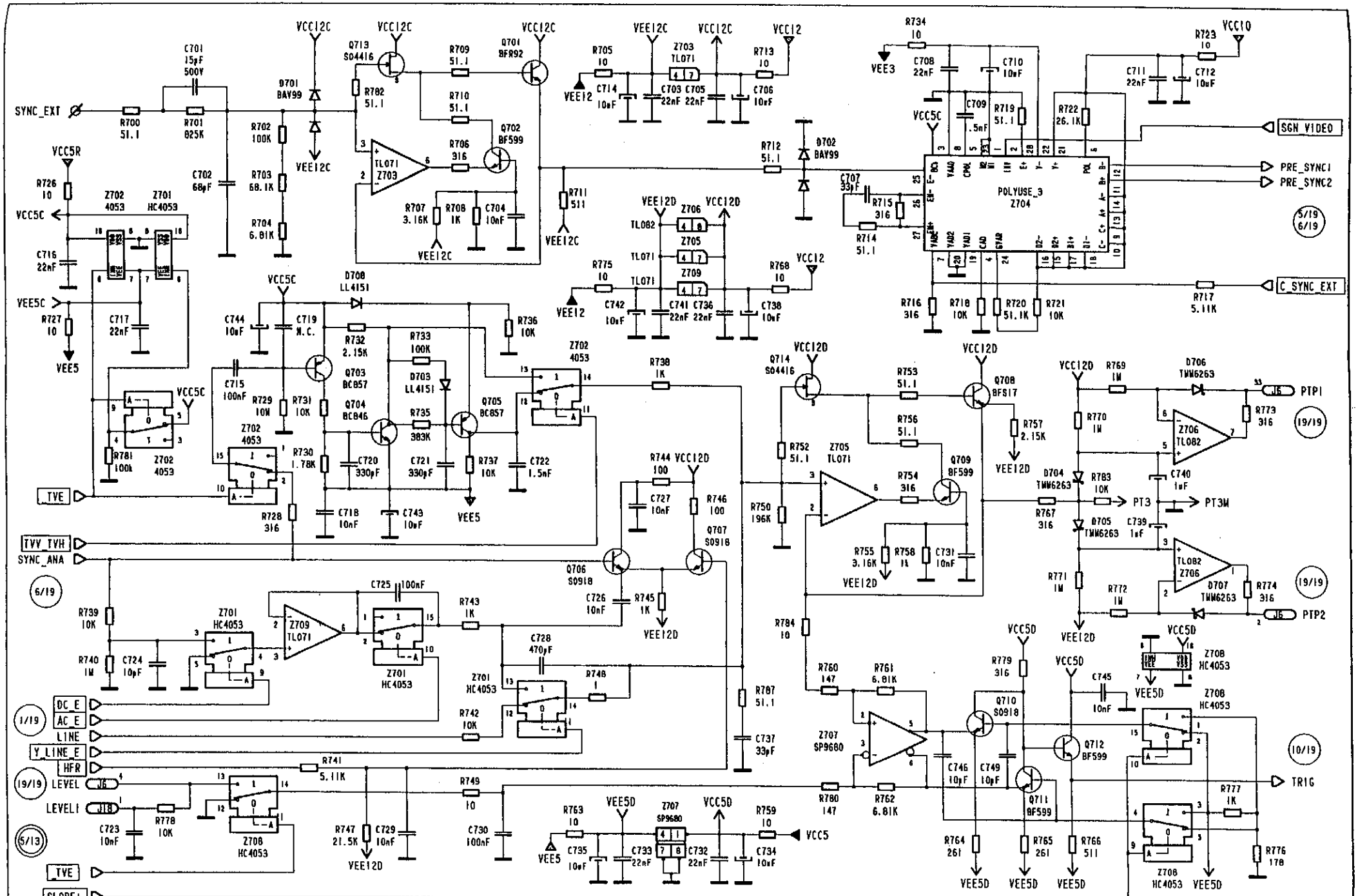

INPUT_CHI
E301
R302 51.1
R301 10K
C353 22nF
D301 100nF
VCC12RA
K301 AI2WK
R307 31.6
C303 6.8pF 500V
C947 15pF 500V
R304 900K 0.5%
R317 40.2
R376 51.1
R308 111K
C306 47pF 500V
C304 2_18p CAPA ENTR.
C305 2_18p REP 1/10
K302 AI2WK
D302 100nF
R318 31.6
C308 2.7pF 500V
C346 15pF 500V
R309 950K 0.5%
C310 2_18p REP 1/200
R321 40.2
R379 51.1
R312 111K
C312 2_18p REP 1/20
C313 47pF 500V
R376 100K
R310 1M
C301 220pF 500V
C322 10pF
R323 511
R370 261
C309 3.9pF
R324 383K
VCC12A
D313 5.1V
Q301 BF992
R306 51.1
C325 10nF
C311 10nF
R344 681
D310 5.1V
Q319 BF599
R328 51.1
Q312 LL4151
Q304 BFS17
C320 470pF
R340 51.1
C323 330pF
C328 N.C.
R347 511
D309 5.1V
C329 10nF
Q307 BFS17
Q306 BFS17
C333 10nF
C332 22nF
Q308 BSD22
C341 10nF
C334 10nF
R358 51.1
ATT_CHI
5/19
C330 N.C.
C335 10nF
Q309 BSD22
Q318 BF599
R325 10W
R339 2.15K
Q305 BFR92
VEE12A
R348 5.11K
R349 1K
R350 1K
R351 10
R352 10
R353 100
R342 51.1K
R343 215
K303 AI2WK
R345 100
C324 22nF 400V
D303 100nF
C352 22nF
K303 AI2WK
HI1_10
R303 5.11K
Q315 BC817
HI1_20
R311 5.11K
Q316 BC817
DC_AC1
R337 5.11K
Q317 BC817
C315 10pF
VEE12A
C317 XXnF
LT1096 Z301
C316 XXnF
R330 1K
Q303 BF599
R322 51.1
R331 2.15K
C356 N.C. (2.2nF)
R333 681
R338 1M
C355 NC
R334 14.7K
R375 8.25K
R346 10K EQUIL. AC/DC1
D307 NC
D311 NC
R354 49.9
Q310 BSD22
C336 10nF
R359 10
R355 10
Q311 BSD22
C337 10nF
R369 51.1
R360 10
Q312 BSD22
R357 40.2
C331 N.C.
C338 10nF
VEE5A
BI1_1
BI1_2
BI1_4
BI1_5
BI1_GND
BI2_GND
VCC12
R364 100K
Z306 LM324D
Z305 TL082
R363 26.1K
B12_GNDB
4/19
R335 1
C319 220nF
C318 22nF
R316 1.47K
C344 22nF
R315 1K
VEE12
R336 10
C327 220nF
C326 22nF
R377 10
C354 47nF
IC 13711
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) ENTREE CHI
DATE 21/09/94
3/19


INPUT_CH2
E401
R402 51.1
R401 10K
C453 22nF
D401 100nF
VCC12RB
K401 A12WK
R407 31.6
C403 6.8pF 500V
R404 900K 0.5%
C446 15pF 500V
C404 2_18p CAPA ENTR.
R479 51.1
R417 40.2
R408 111K
C406 47pF 500V
C405 2_18p REP 1/10
C452 22nF
D402 100nF
K402 A12WK
C410 2_18p REP 1/200
R418 31.6
C408 2.7pF 500V
R409 950K 0.5%
C447 15pF 500V
R420 40.2
R480 51.1
R412 111K
C412 2_18p REP 1/20
R476 100K
C413 47pF 500V
R410 1M
R426 10M
C401 220pF 500V
R470 261
C409 3.9pF
C426 10pF
R424 511
R406 51.1
D413 5.1V
R425 383K
Q403 BF992
C439 10nF
C411 10nF
R448 681
D410 5.1V
C433 10nF
C432 22nF
Q411 BFS17
D409 5.1V
Q408 BFS17
Q419 BF599
C422 470pF
R429 51.1
D412 LL4151
R436 51.1
C427 330pF
C428 1.8pF
R437 51.1K
R438 215
R446 2.15K
VEE12B
BF599 Q418
Q409 BFR92
C429 10nF
R449 511
Q410 BFS17
R454 10
R457 10
Q412 BSD22
C441 10nF
C434 10nF
R463 51.1
ATT_CH2
6/19
Q413 BSD22
C430 N.C.
C435 10nF
R450 5.11K
R455 1K
R456 1K
R458 100
VEE12B
R459 49.9
Q414 BSD22
C436 10nF
R464 10
R460 10
Q415 BSD22
C437 10nF
R465 10
R474 51.1
Q416 BSD22
VEE5B
R461 40.2
C431 N.C.
C438 10nF
HI2_10
R403 5.11K
Q401 BC817
HI2_20
R411 5.11K
Q402 BC817
DC_AC2
R447 5.11K
Q417 BC817
VCC12RB2
D403 100nF
C451 22nF
K403 A12WK
K403 A12WK
R413 100
C424 22nF 400V
C415 10pF
VEE12B
C417 XXnF
LT1096 Z401
C416 XXnF
VCC12B
R431 1K
Q407 BF599
R405 51.1
R432 2.15K
C457 N.C. (2.2nF)
R440 681
VEE12B
VEE12B
VEE12B
C456 NC
R441 14.7K
R475 1M
R434 8.25K
R439 10K EQUIL. AC/DC2
D407 NC
D411 NC
BI2_1
BI2_2
BI2_4
BI2_5
BI2_GNDB
VCC12
R467 100K
Z406 LM324D
R466 26.1K
3/19
R416 1.47K
C445 22nF
R415 1K
VEE5B
VEE12
R435 10
C421 220nF
C420 22nF
VEE12B
VEE12
VCC12
VCC12B
R423 1
C419 220nF
C418 22nF
R477 10
VCC12
VCC12RB
C454 47nF
R478 10
VCC12
VCC12RB2
C455 47nF
VCC12
LM3240 Z406
VEE12
IC 13712
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) ENTREE CH2
DATE 21/09/94
4/19

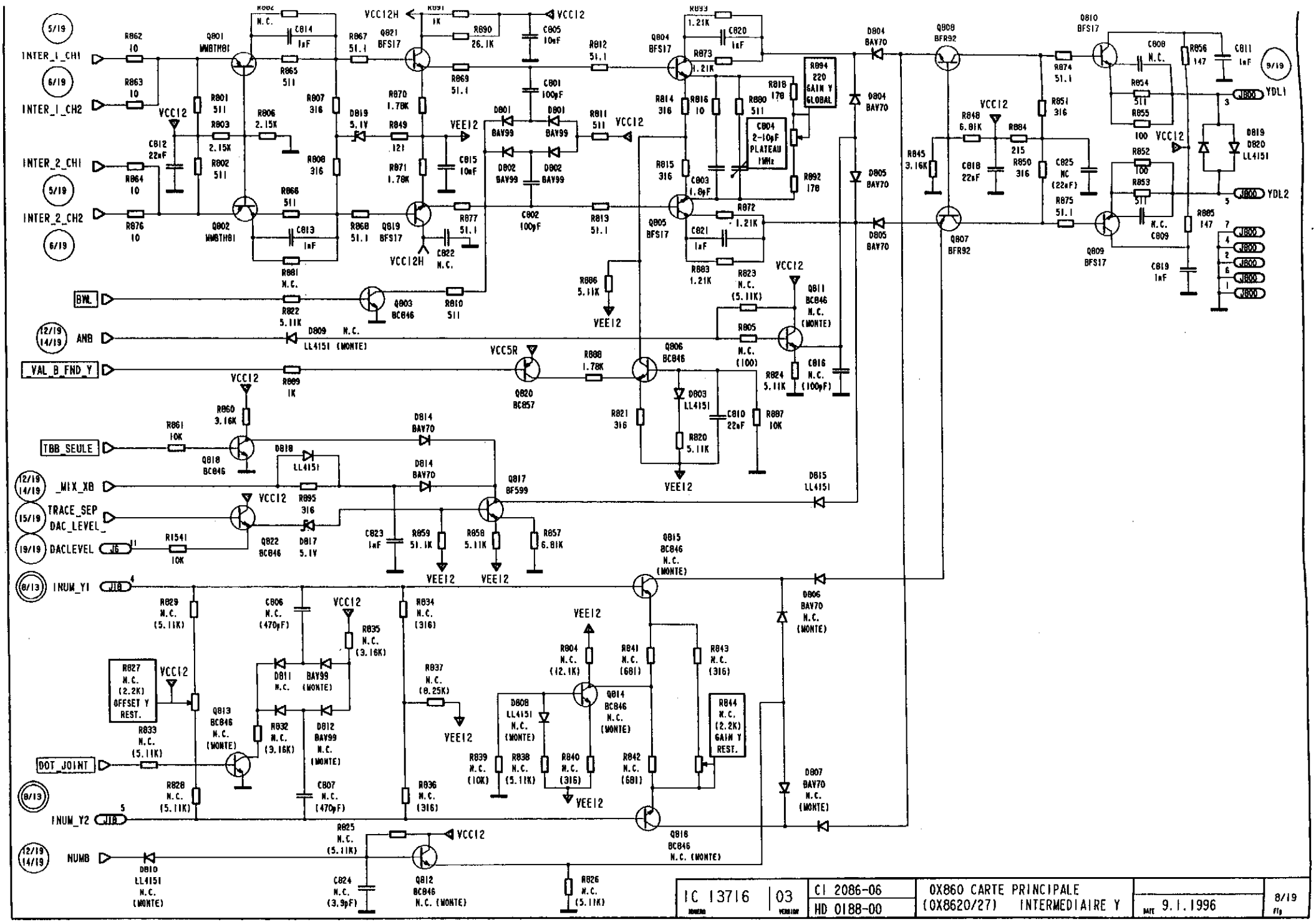


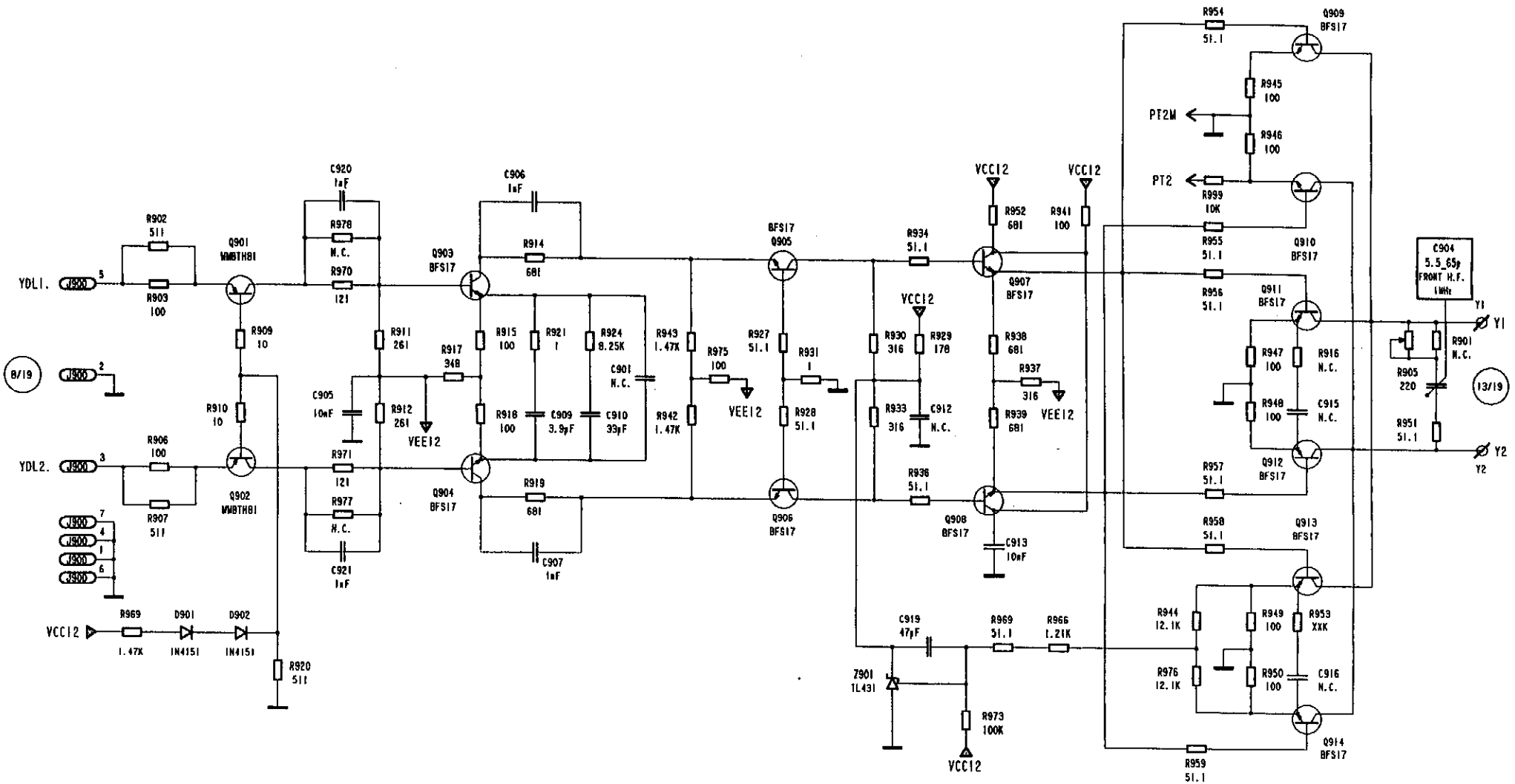
IC 13713	03	CI 2086-05.1	0X860 CARTE PRINCIPALE		5/19
		HD 0188-00	(0X8620/27) MUX. CH1	8.1.1996	


INTER_2_CH2
INTER_1_CH2
PRE_NUM2_2
PRE_NUM2_1
SYNC_ANA
PRE_SYNC1
PRE_SYNC2
VOS_SYNC1
VOS_SYNC2_EXT
VAL_PRE_SY1
VAR_CH2
VAR_ADJ2
VOS_DEC2
CAD_CH2
VAL_CAD_CH2
VAL_PRE_SY2
SGN_VIDEO
VALID_CH2
VOS_MUX2
VAL_INV_2
ATT_CH2
GY2X2_5
VCC12
VEE12
VCC10
VCC10B
VEE3
VCC5R
Z601 POLYUSE_3
Z602 4053
Z603 TL082
Z604 TL082
IC 13714
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) MUX. CH2
21/09/94
6/19



IC 13715	03	CI 2086-05.1	0X860 CARTE PRINCIPALE		7/19
		HD 0188-00	(0X8620/27) TRIGGER	DATE 9.1.1996	


INTER_1_CH1
INTER_1_CH2
INTER_2_CH1
INTER_2_CH2
BWL
ANB
_VAL_B_FND_Y
TBB_SEULE
_MIX_XB
TRACE_SEP
DAC_LEVEL_
DACLEVEL
INUM_Y1
INUM_Y2
DOT_JOINT
NUMB
YDL1
YDL2
VCC12
VCC12H
VCC5R
VEE12
Q801 MMBTH81
Q802 MMBTH81
Q803 BC846
Q804 BFS17
Q805 BFS17
Q806 BC846
Q807 BFR92
Q808 BFR92
Q809 BFS17
Q810 BFS17
Q811 BC846 N.C. (MONTE)
Q812 BC846 N.C. (MONTE)
Q813 BC846 N.C. (MONTE)
Q814 BC846 N.C. (MONTE)
Q815 BC846 N.C. (MONTE)
Q816 BC846 N.C. (MONTE)
Q817 BF599
Q818 BC846
Q819 BFS17
Q820 BC857
Q821 BFS17
Q822 BC846
R801 511
R802 511
R803 2.15K
R804 .121
R805 N.C. (100)
R806 2.15K
R807 316
R808 316
R809 1K
R810 511
R811 511
R812 51.1
R813 51.1
R814 316
R815 316
R816 10
R817 1.21K
R818 178
R820 5.11K
R821 316
R822 5.11K
R823 N.C. (5.11K)
R824 5.11K
R825 N.C. (5.11K)
R826 N.C. (5.11K)
R827 N.C. (2.2K) OFFSET Y REST.
R828 N.C. (5.11K)
R829 N.C. (5.11K)
R830 N.C. (10K)
R831 N.C. (5.11K)
R832 N.C. (3.16K)
R833 N.C. (5.11K)
R834 N.C. (316)
R835 N.C. (3.16K)
R836 N.C. (316)
R837 N.C. (8.25K)
R838 N.C. (5.11K)
R839 N.C. (10K)
R840 N.C. (316)
R841 N.C. (681)
R842 N.C. (681)
R843 N.C. (316)
R844 N.C. (2.2K) GAIN Y REST.
R845 3.16K
R848 6.81K
R850 316
R851 316
R852 100
R853 511
R854 511
R855 100
R856 147
R857 6.81K
R858 5.11K
R859 51.1K
R860 3.16K
R861 10K
R862 10
R863 10
R864 10
R865 511
R866 511
R867 51.1
R868 51.1
R869 51.1
R870 1.78K
R871 1.78K
R872 1.21K
R873 1.21K
R874 51.1
R875 51.1
R876 10
R877 51.1
R880 511
R881 N.C.
R882 N.C.
R883 1.21K
R884 215
R885 147
R886 5.11K
R887 10K
R888 1.78K
R889 1K
R890 26.1K
R891 1K
R892 178
R893 1.21K
R894 220 GAIN Y GLOBAL
R895 316
R1541 10K
C801 100pF
C802 100pF
C803 1.8pF
C804 2-10pF PLATEAU 1MHz
C805 10nF
C806 N.C. (470pF)
C807 N.C. (470pF)
C808 N.C.
C809 N.C.
C810 22nF
C811 1nF
C812 22nF
C813 1nF
C814 1nF
C815 10nF
C816 N.C. (100pF)
C817 1nF
C818 22nF
C819 1nF
C820 1nF
C821 1nF
C822 N.C.
C823 1nF
C824 N.C. (3.9pF)
C825 NC (22nF)
D801 BAY99
D802 BAY99
D803 LL4151
D804 BAY70
D805 BAY70
D806 BAY70 N.C. (MONTE)
D807 BAY70 N.C. (MONTE)
D808 LL4151 N.C. (MONTE)
D809 N.C. LL4151 (MONTE)
D810 LL4151 N.C. (MONTE)
D811 N.C. BAY99 (MONTE)
D812 BAY99 N.C. (MONTE)
D814 BAY70
D815 LL4151
D817 5.1V
D818 LL4151
D819 5.1V
D819 D820 LL4151
J6
J16
J800
5/19
6/19
12/19 14/19
15/19
19/19
8/13
9/19
IC 13716
03
CI 2086-06
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) INTERMEDIAIRE Y
DATE 9.1.1996
8/19



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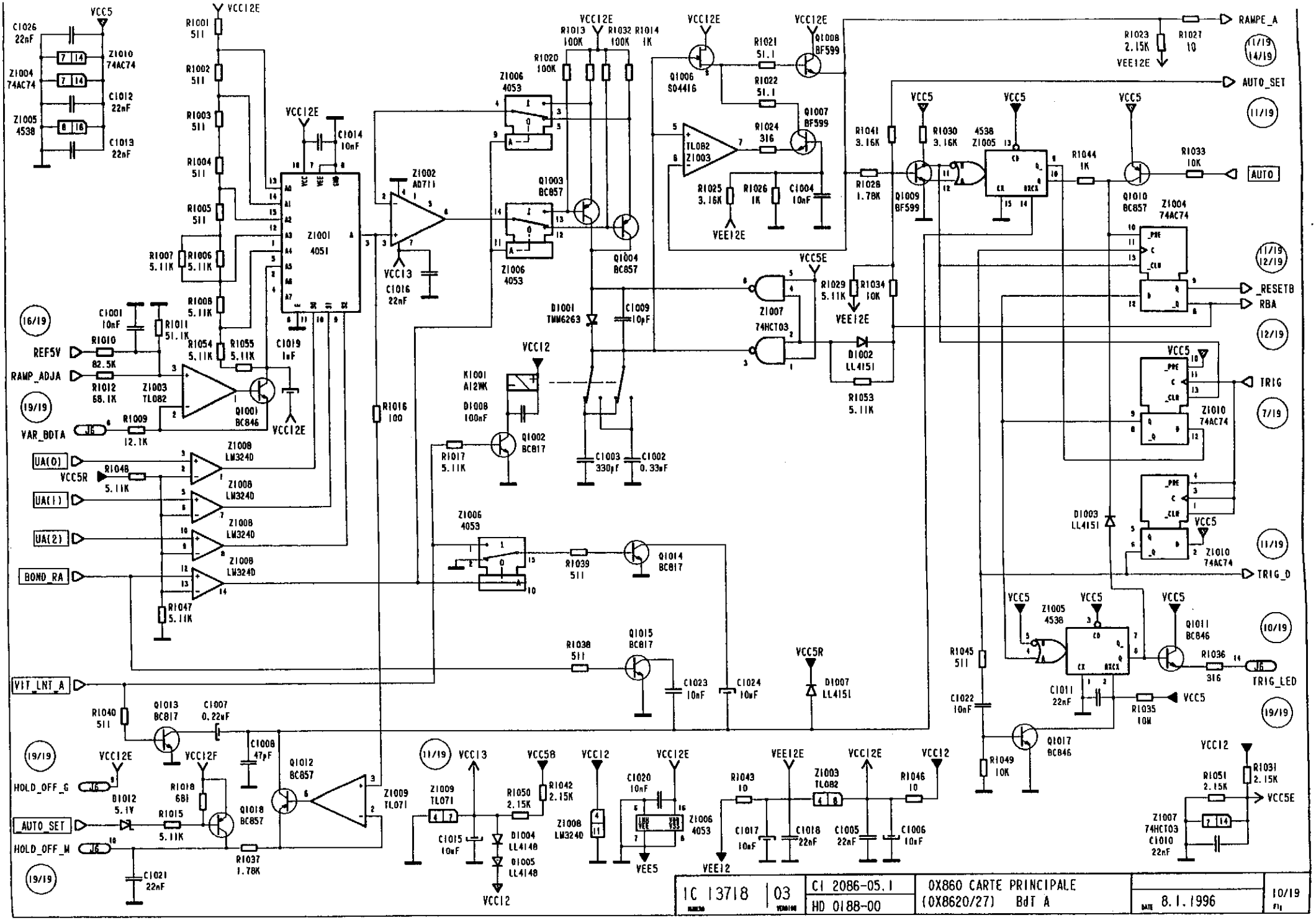
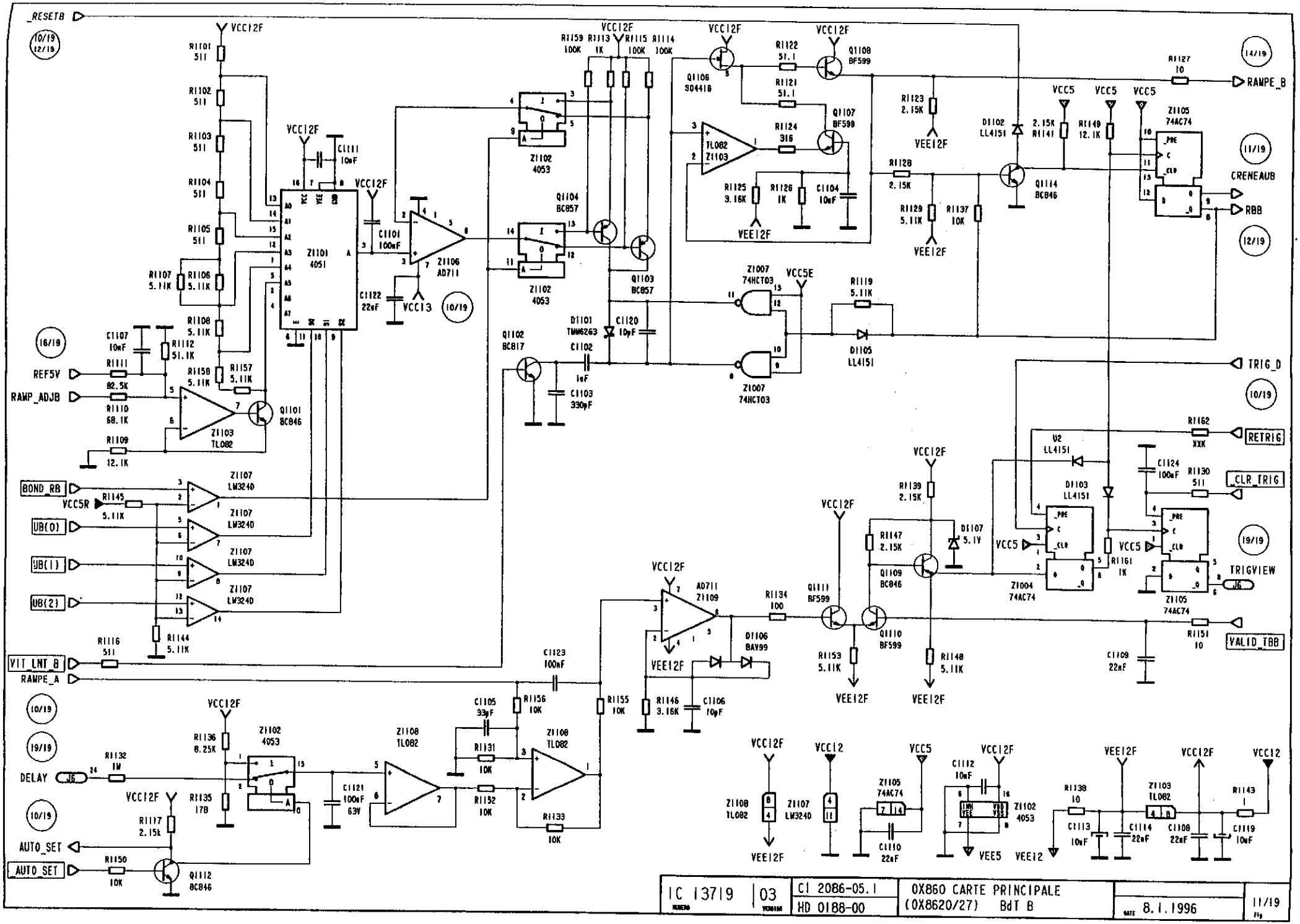
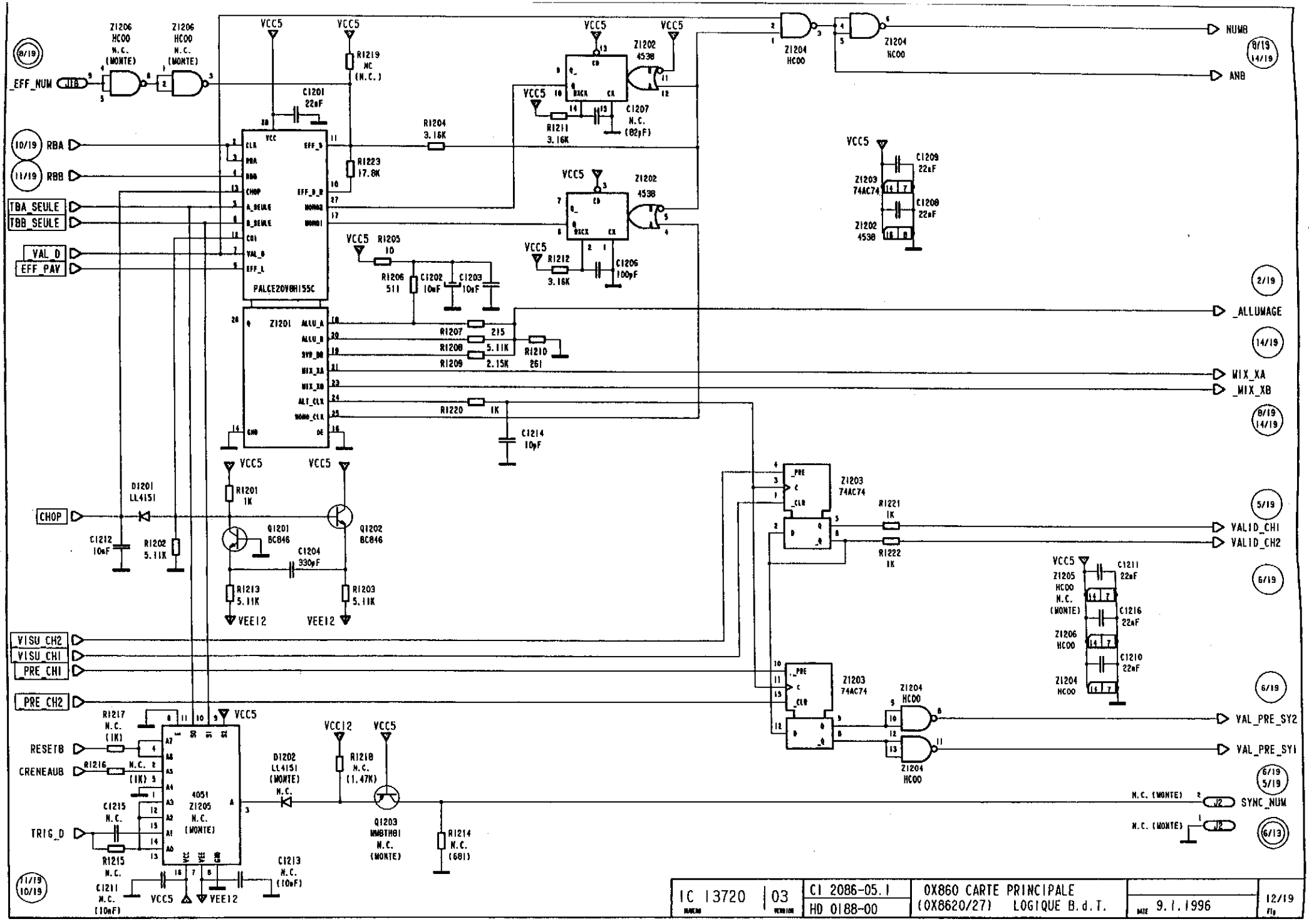
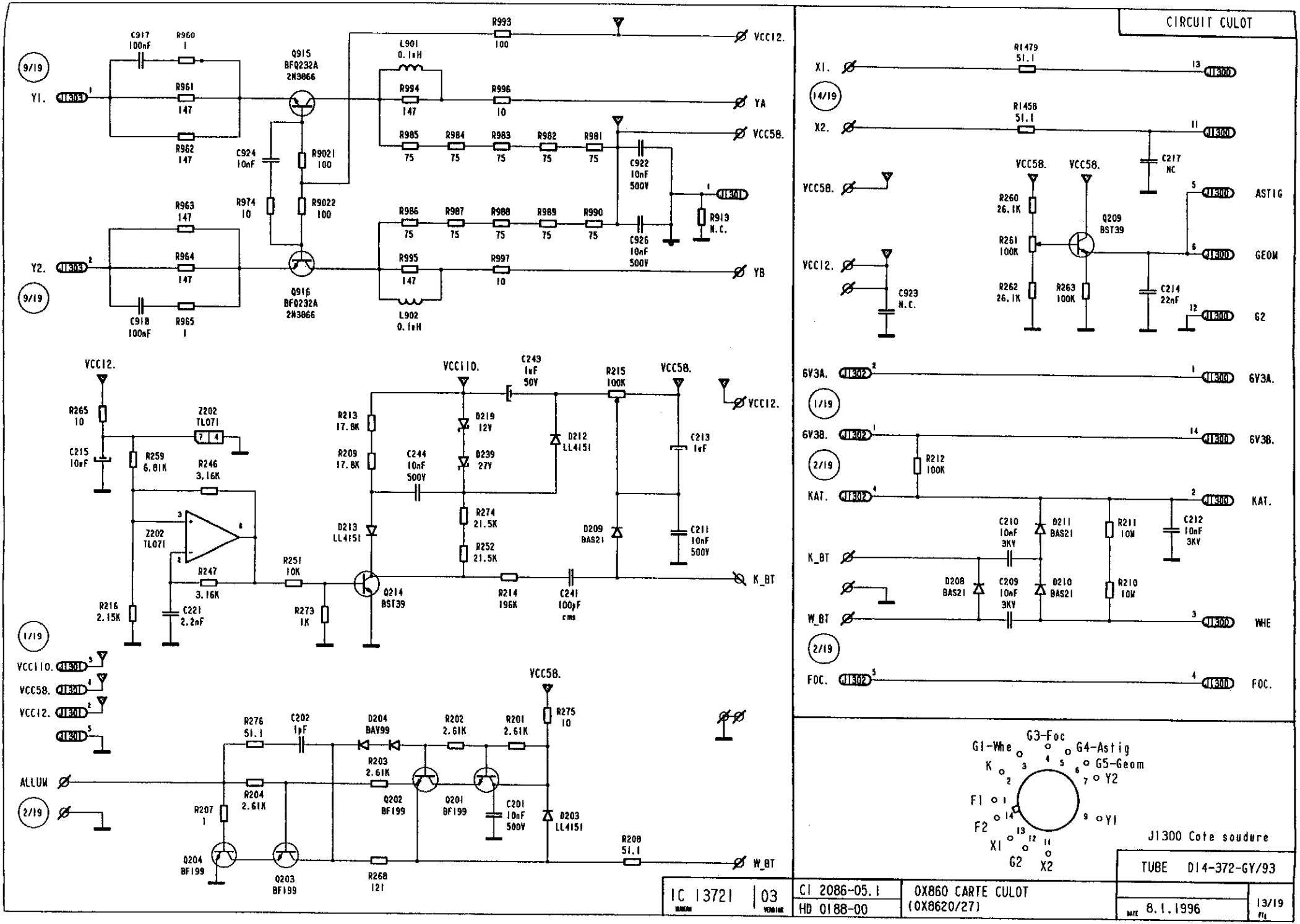
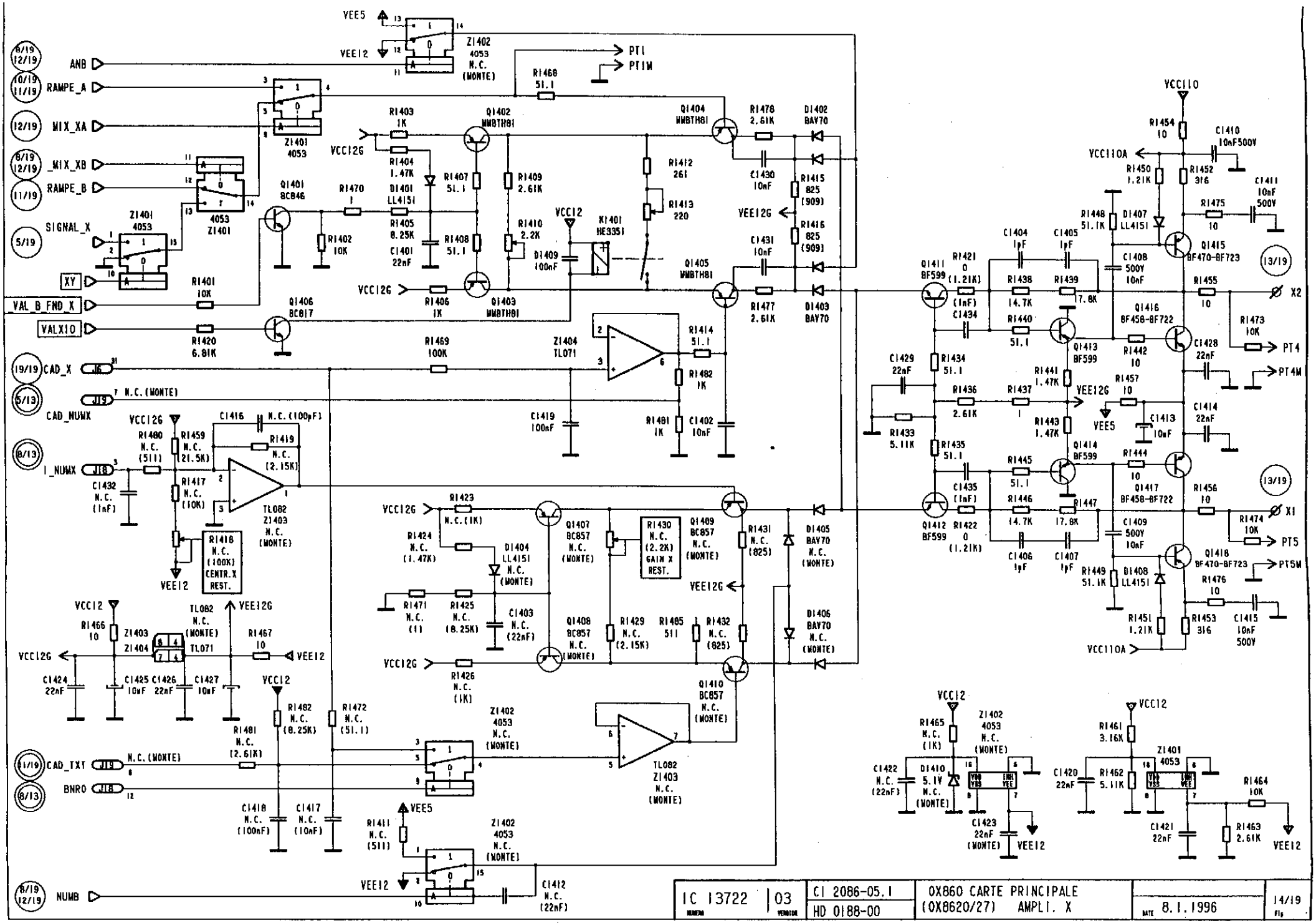
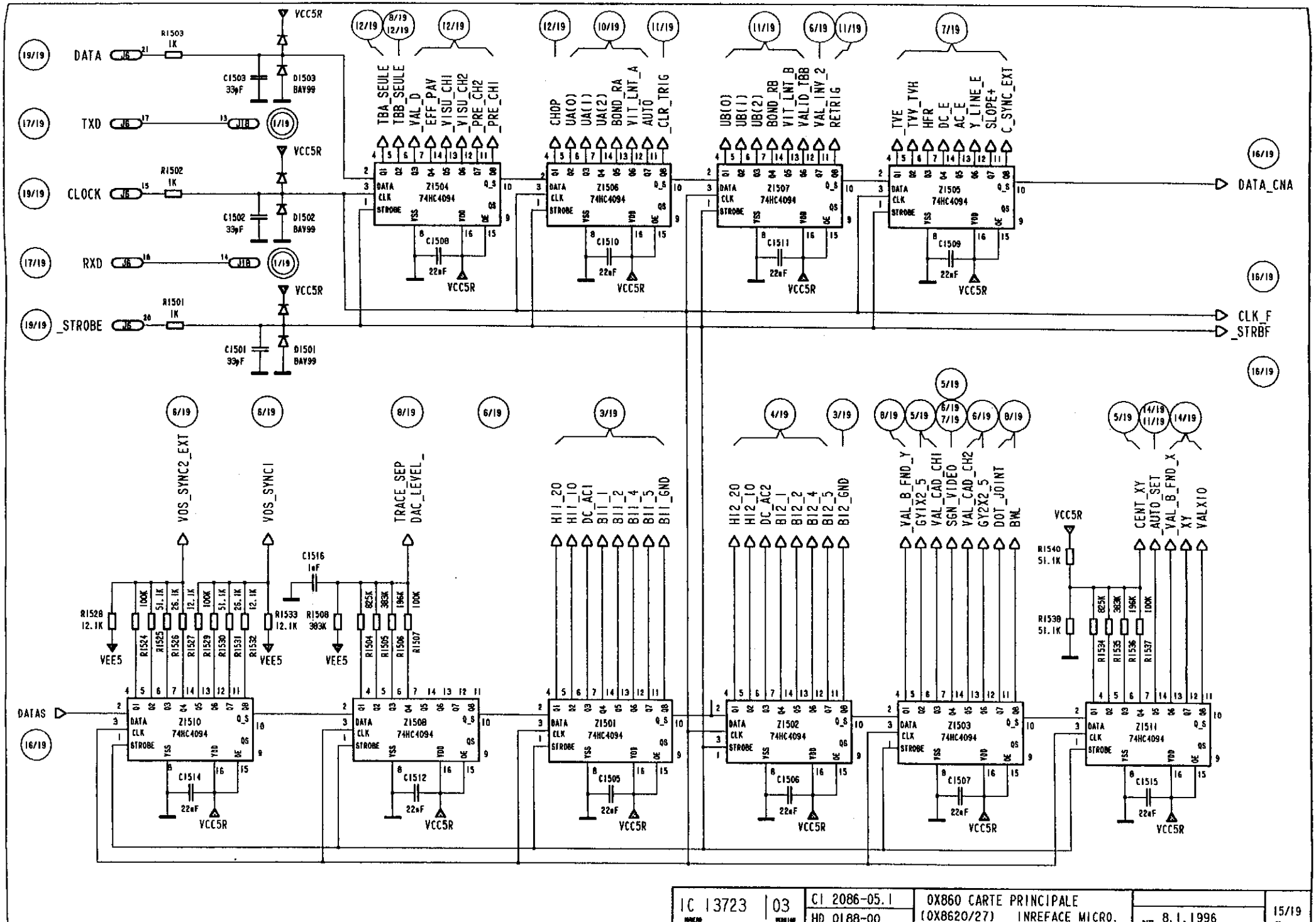

VCC5
VCC12E
VCC5R
VCC5E
VCC12
VCC13
VCC12F
VCC58
VEE12E
VEE5
C1026 22nF
Z1010 74AC74
Z1004 74AC74
C1012 22nF
Z1005 4538
C1013 22nF
R1001 511
R1002 511
R1003 511
R1004 511
R1005 511
R1007 5.11K
R1006 5.11K
R1008 5.11K
C1014 10nF
Z1001 4051
Z1002 AD711
VCC13
C1016 22nF
C1001 10nF
R1011 51.1K
R1010 82.5K
R1054 5.11K
R1055 5.11K
C1019 1nF
REF5V
RAMP_ADJA
R1012 68.1K
Z1003 TL082
Q1001 BC846
VAR_BDTA
R1009 12.1K
R1016 100
UA(0)
UA(1)
UA(2)
BOND_RA
R1048 5.11K
Z1008 LM324D
R1047 5.11K
VIT_LNT_A
R1040 511
Q1013 BC817
C1007 0.22uF
C1008 47pF
Q1012 BC857
Z1009 TL071
HOLD_OFF_G
D1012 5.1V
AUTO_SET
R1015 5.11K
R1018 681
Q1018 BC857
HOLD_OFF_M
R1037 1.78K
C1021 22nF
R1013 100K
R1032 100K
R1014 1K
R1020 100K
Z1006 4053
Q1003 BC857
Q1004 BC857
D1001 TMM6263
C1009 10pF
K1001 A12WK
D1008 100nF
Q1002 BC817
R1017 5.11K
C1003 330pF
C1002 0.33nF
R1039 511
Q1014 BC817
R1038 511
Q1015 BC817
C1023 10nF
C1024 10nF
D1007 LL4151
C1015 10nF
D1004 LL4148
D1005 LL4148
R1050 2.15K
R1042 2.15K
C1020 10nF
R1043 10
R1046 10
C1017 10nF
C1018 22nF
C1005 22nF
C1006 10nF
Q1006 S04416
R1021 51.1
R1022 51.1
Q1008 BF599
Q1007 BF599
R1024 316
TL082 Z1003
R1025 3.16K
R1026 1K
C1004 10nF
R1041 3.16K
R1030 3.16K
R1028 1.78K
Q1009 BF599
Z1007 74HCT03
R1029 5.11K
R1034 10K
D1002 LL4151
R1053 5.11K
R1023 2.15K
R1027 10
RAMPE_A
AUTO_SET
R1044 1K
R1033 10K
AUTO
Q1010 BC857
_RESETB
RBA
TRIG
TRIG_D
D1003 LL4151
R1045 511
C1022 10nF
Q1017 BC846
R1049 10K
Q1011 BC846
R1036 316
TRIG_LED
C1011 22nF
R1035 10K
R1031 2.15K
R1051 2.15K
C1010 22nF
IC 13718
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) BdT A
8.1.1996
10/19

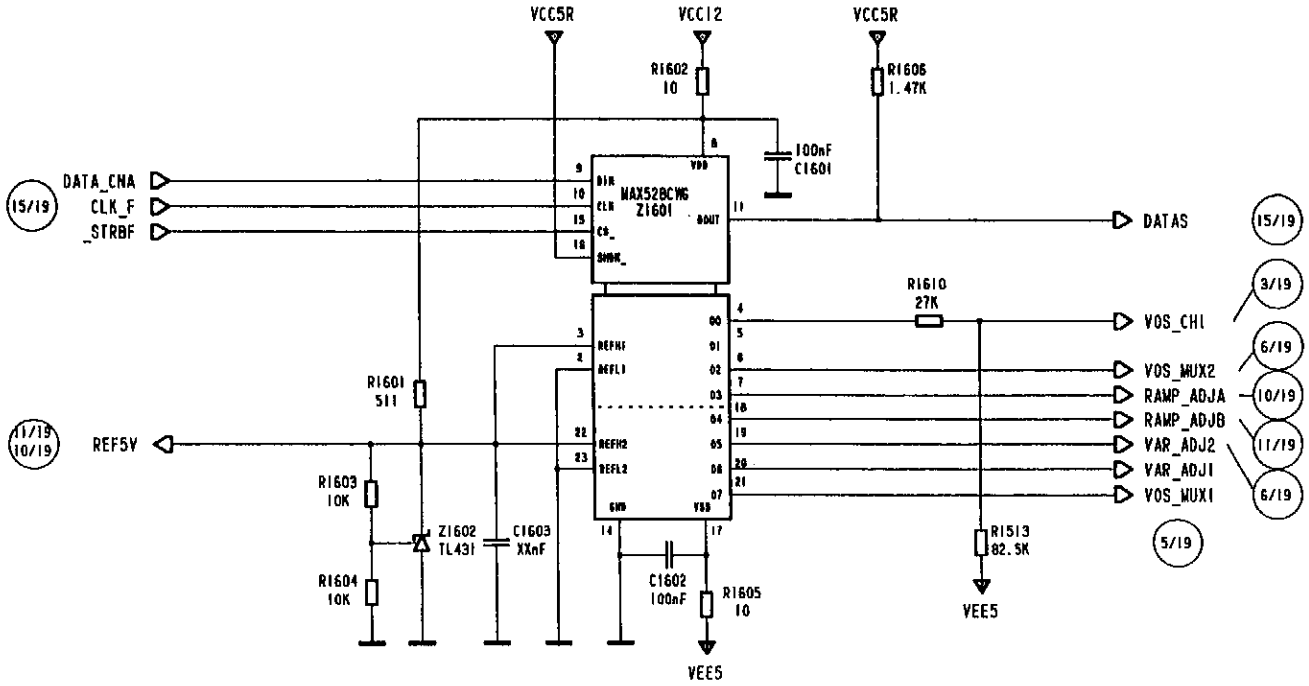

_RESETB
VCC12F
VCC5
VCC5R
VCC5E
VCC13
VEE12F
VCC12
VEE12
VEE5
R1101 511
R1102 511
R1103 511
R1104 511
R1105 511
R1106 5.11K
R1107 5.11K
R1108 5.11K
R1109 12.1K
R1110 68.1K
R1111 82.5K
R1112 51.1K
R1113 1K
R1114 100K
R1115 100K
R1116 511
R1117 2.15k
R1118 10K
R1119 5.11K
R1120 10K
R1121 51.1
R1122 51.1
R1123 2.15K
R1124 316
R1125 3.16K
R1126 1K
R1127 10
R1128 2.15K
R1129 5.11K
R1130 511
R1131 10K
R1132 1M
R1133 10K
R1134 100
R1135 178
R1136 8.25K
R1137 10K
R1138 10
R1139 2.15K
R1141 2.15K
R1143 1
R1144 5.11K
R1145 5.11K
R1146 3.16K
R1147 2.15K
R1148 5.11K
R1149 12.1K
R1150 10K
R1151 10
R1152 10K
R1153 5.11K
R1155 10K
R1156 10K
R1157 5.11K
R1158 5.11K
R1161 1K
R1162 XXK
C1101 100nF
C1102 1nF
C1103 330pF
C1104 10nF
C1105 33pF
C1106 10pF
C1107 10nF
C1108 22nF
C1109 22nF
C1110 22nF
C1111 10nF
C1112 10nF
C1113 10nF
C1114 22nF
C1119 10nF
C1120 10pF
C1121 100nF 63V
C1122 22nF
C1123 100nF
C1124 100nF
C1125 22nF
Z1101 4051
Z1102 4053
Z1103 TL082
Z1104 74AC74
Z1105 74AC74
Z1106 AD711
Z1107 LM3240
Z1108 TL082
Z1109 AD711
Z1004 74AC74
Z1007 74HCT03
Q1101 BC846
Q1102 BC817
Q1103 BC857
Q1104 BC857
Q1105 S04416
Q1106 S04416
Q1107 BF599
Q1108 BF599
Q1109 BC846
Q1110 BF599
Q1111 BF599
Q1112 BC846
Q1113 BC846
D1101 TMM6263
D1102 LL4151
D1103 LL4151
D1104 LL4151
D1105 LL4151
D1106 BAV99
D1107 5.1V
BOND_RB
UB(0)
UB(1)
UB(2)
VIT_LNT_B
RAMPE_A
DELAY
AUTO_SET
_AUTO_SET
REF5V
RAMP_ADJB
RAMPE_B
CRENEAUB
RBB
TRIG_D
RETRIG
_CLR_TRIG
TRIGVIEW
VALID_TBB
J6
10/19
12/19
14/19
11/19
12/19
16/19
10/19
19/19
IC 13719
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) BdT B
DATE 8.1.1996
11/19


Z1206 HC00 N.C. (MONTE)
Z1206 HC00 N.C. (MONTE)
_EFF_NUM
R1219 NC (N.C.)
C1201 22nF
R1204 3.16K
R1223 17.8K
Z1202 4538
C1207 N.C. (82pF)
R1211 3.16K
Z1204 HC00
Z1204 HC00
NUMB
ANB
RBA
RBB
TBA_SEULE
TBB_SEULE
VAL_D
EFF_PAV
PALCE20V8H15SC
R1205 10
R1206 511
C1202 10nF
C1203 10nF
R1212 3.16K
C1206 100pF
C1209 22nF
Z1203 74AC74
C1208 22nF
_ALLUMAGE
Z1201
R1207 215
R1208 5.11K
R1209 2.15K
R1210 261
MIX_XA
_MIX_XB
R1220 1K
C1214 10pF
CHOP
D1201 LL4151
C1212 10nF
R1202 5.11K
R1201 1K
Q1201 BC846
Q1202 BC846
C1204 330pF
R1213 5.11K
R1203 5.11K
VEE12
Z1203 74AC74
R1221 1K
R1222 1K
VALID_CH1
VALID_CH2
C1211 22nF
Z1205 HC00 N.C. (MONTE)
C1216 22nF
Z1206 HC00
C1210 22nF
Z1204 HC00
VISU_CH2
VISU_CH1
PRE_CH1
PRE_CH2
R1217 N.C. (1K)
RESETB
CRENEAUB
R1216 N.C. (1K)
4051 Z1205 N.C. (MONTE)
C1215 N.C.
TRIG_D
R1215 N.C.
C1211 N.C. (10nF)
C1213 N.C. (10nF)
D1202 LL4151 (MONTE) N.C.
R1218 N.C. (1.47K)
Q1203 MMBTH81 N.C. (MONTE)
R1214 N.C. (68)
VAL_PRE_SY2
VAL_PRE_SY1
N.C. (MONTE)
SYNC_NUM
IC 13720
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) LOGIQUE B.d.T.
9.1.1996
12/19


CIRCUIT CULOT
C917 100nF
R960 1
R961 147
R962 147
Q915 BFQ232A 2N3866
L901 0.1uH
R993 100
VCC12.
R994 147
R996 10
YA
VCC58.
R985 75
R984 75
R983 75
R982 75
R981 75
C922 10nF 500V
C924 10nF
R9021 100
R974 10
R9022 100
J1301
R913 N.C.
R963 147
R964 147
R965 1
C918 100nF
Q916 BFQ232A 2N3866
L902 0.1uH
R986 75
R987 75
R988 75
R989 75
R990 75
C926 10nF 500V
R995 147
R997 10
YB
Y1. J1303
Y2. J1303
9/19
R1479 51.1
R1458 51.1
X1.
X2.
14/19
J1300
C217 NC
R260 26.1K
R261 100K
R262 26.1K
R263 100K
Q209 BST39
C214 22nF
ASTIG
GEOM
G2
C923 N.C.
6V3A. J1302
6V3B. J1302
1/19
2/19
R212 100K
KAT. J1302
K_BT
W_BT
FOC. J1302
C210 10nF 3KV
D211 BAS21
R211 10M
C212 10nF 3KV
D208 BAS21
C209 10nF 3KV
D210 BAS21
R210 10M
6V3A.
6V3B.
KAT.
WHE
FOC.
VCC12.
R265 10
Z202 TL071
C215 10nF
R259 6.81K
R246 3.16K
R247 3.16K
R216 2.15K
C221 2.2nF
R251 10K
R273 1K
Q214 BST39
VCC110.
C243 1uF 50V
R215 100K
R213 17.8K
R209 17.8K
D219 12V
D239 27V
C244 10nF 500V
D212 LL4151
C213 1uF
R274 21.5K
R252 21.5K
D213 LL4151
D209 BAS21
C211 10nF 500V
R214 196K
C241 100pF cms
VCC110.
VCC58.
VCC12.
J1301
ALLUM
R276 51.1
C202 1pF
D204 BAY99
R202 2.61K
R201 2.61K
R275 10
R203 2.61K
R204 2.61K
R207 1
Q202 BF199
Q201 BF199
C201 10nF 500V
D203 LL4151
Q204 BF199
Q203 BF199
R268 121
R208 51.1
G3-Foc
G1-Whe
G4-Astig
G5-Geom
K
Y2
F1
Y1
F2
X1
G2
X2
J1300 Cote soudure
TUBE D14-372-GY/93
IC 13721
03
CI 2086-05.1
HD 0188-00
0X860 CARTE CULOT
(0X8620/27)
DATE 8.1.1996
13/19


ANB
RAMPE_A
MIX_XA
_MIX_XB
RAMPE_B
SIGNAL_X
XY
VAL_B_FND_X
VALX10
CAD_X
CAD_NUMX
I_NUMX
CAD_TXT
BNRO
NUMB
PT1
PT1M
VCC12G
VEE12G
VCC12
VEE12
VEE5
VCC110
VCC110A
X2
X1
PT4
PT4M
PT5
PT5M
TL082
TL071
4053
N.C. (MONTE)
GAIN X REST.
CENTR.X REST.
IC 13722
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) AMPLI. X
8.1.1996
14/19


DATA
TXD
CLOCK
RXD
_STROBE
VCC5R
R1503 1K
R1502 1K
R1501 1K
C1503 33pF
C1502 33pF
C1501 33pF
D1503 BAY99
D1502 BAY99
D1501 BAY99
TBA_SEULE
TBB_SEULE
VAL_D
EFF_PAV
VISU_CHI
VISU_CH2
PRE_CH2
PRE_CHI
CHOP
UA(0)
UA(1)
UA(2)
BOND_RA
VIT_LNT_A
AUTO
CLR_TRIG
UB(0)
UB(1)
UB(2)
BOND_RB
VIT_LNT_B
VALID_TBB
VAL_INV_2
RETRIG
TVE
TVV_TVH
HFR
DC_E
AC_E
Y_LINE_E
SLOPE+
C_SYNC_EXT
Z1504 74HC4094
Z1506 74HC4094
Z1507 74HC4094
Z1505 74HC4094
C1508 22nF
C1510 22nF
C1511 22nF
C1509 22nF
DATA_CNA
CLK_F
_STRBF
VOS_SYNC2_EXT
VOS_SYNCI
TRACE_SEP
DAC_LEVEL_
HI1_20
HI1_10
DC_AC1
BI1_1
BI1_2
BI1_4
BI1_5
BI1_GND
HI2_20
HI2_10
DC_AC2
BI2_1
BI2_2
BI2_4
BI2_5
BI2_GND
VAL_B_FND_Y
GY1X2_5
VAL_CAD_CHI
SGN_VIDEO
VAL_CAD_CH2
GY2X2_5
DOT_JOINT
BWL
CENT_XY
AUTO_SET
VAL_B_FND_X
XY
VALX10
R1528 12.1K
R1533 12.1K
R1508 383K
R1540 51.1K
R1539 51.1K
C1516 1nF
VEE5
Z1510 74HC4094
Z1508 74HC4094
Z1501 74HC4094
Z1502 74HC4094
Z1503 74HC4094
Z1511 74HC4094
C1514 22nF
C1512 22nF
C1505 22nF
C1506 22nF
C1507 22nF
C1515 22nF
DATAS
IC 13723
03
CI 2086-05.1
HD 0188-00
0X860 CARTE PRINCIPALE
(0X8620/27) INREFACE MICRO.
8.1.1996
15/19



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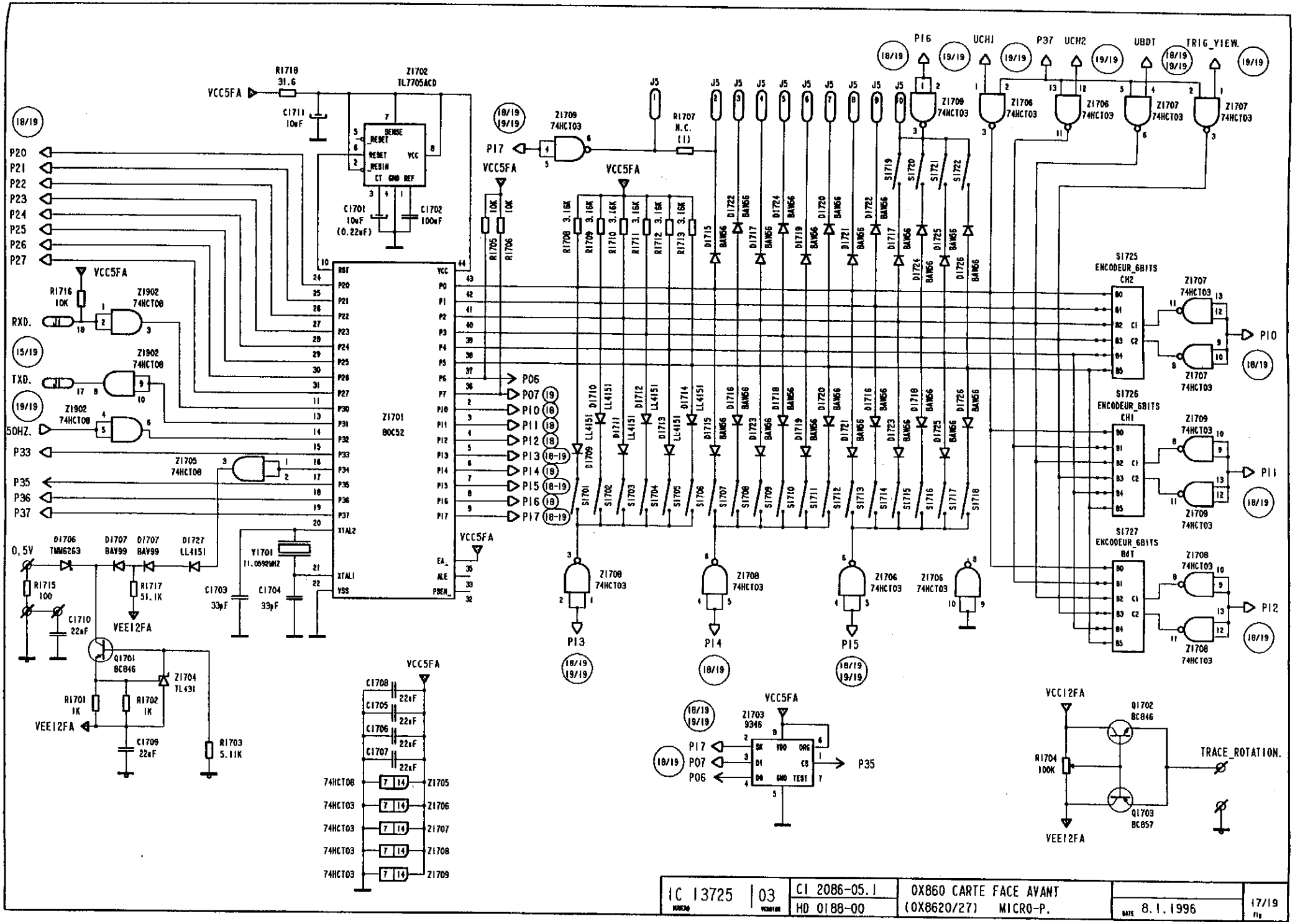
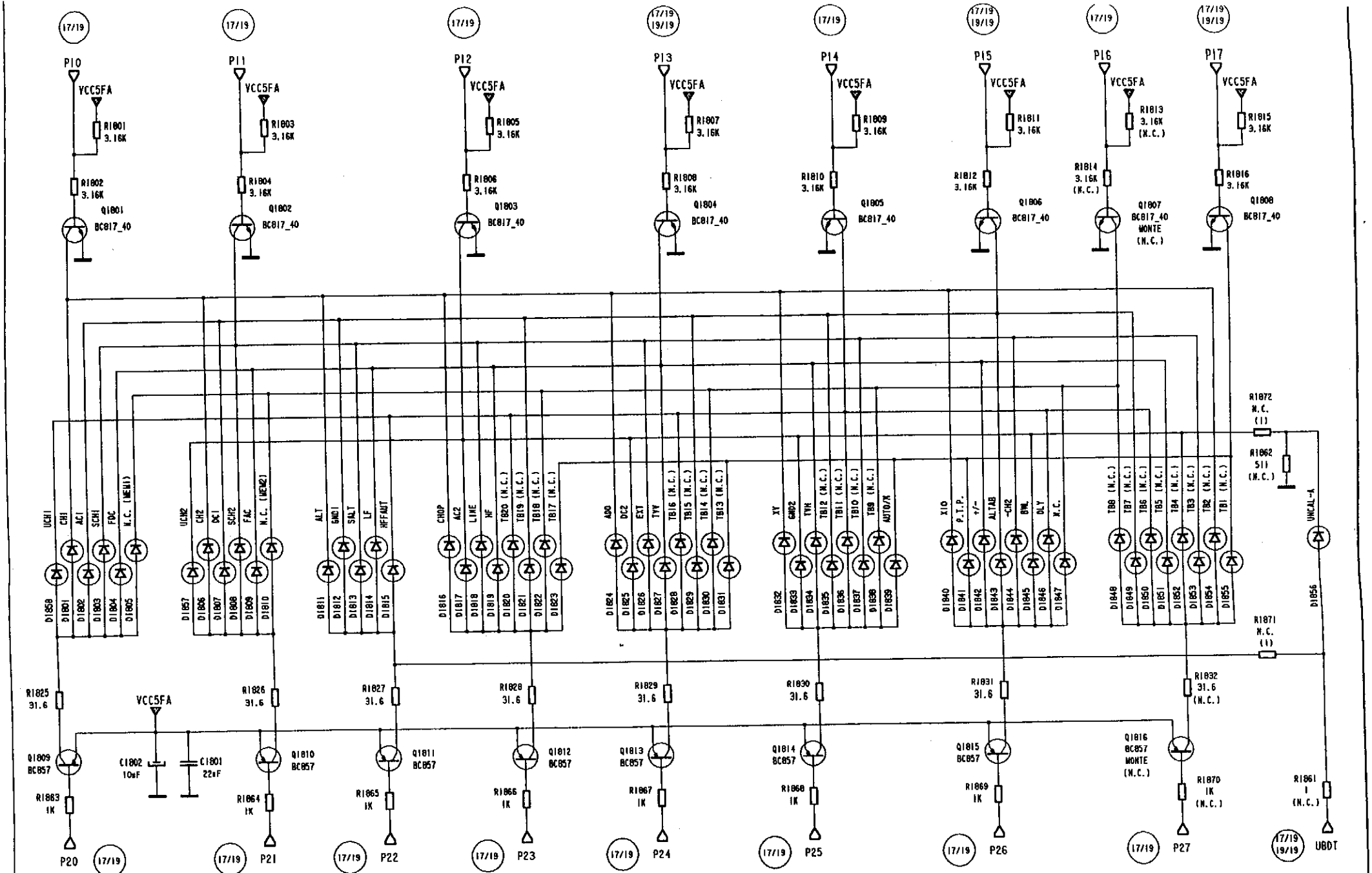
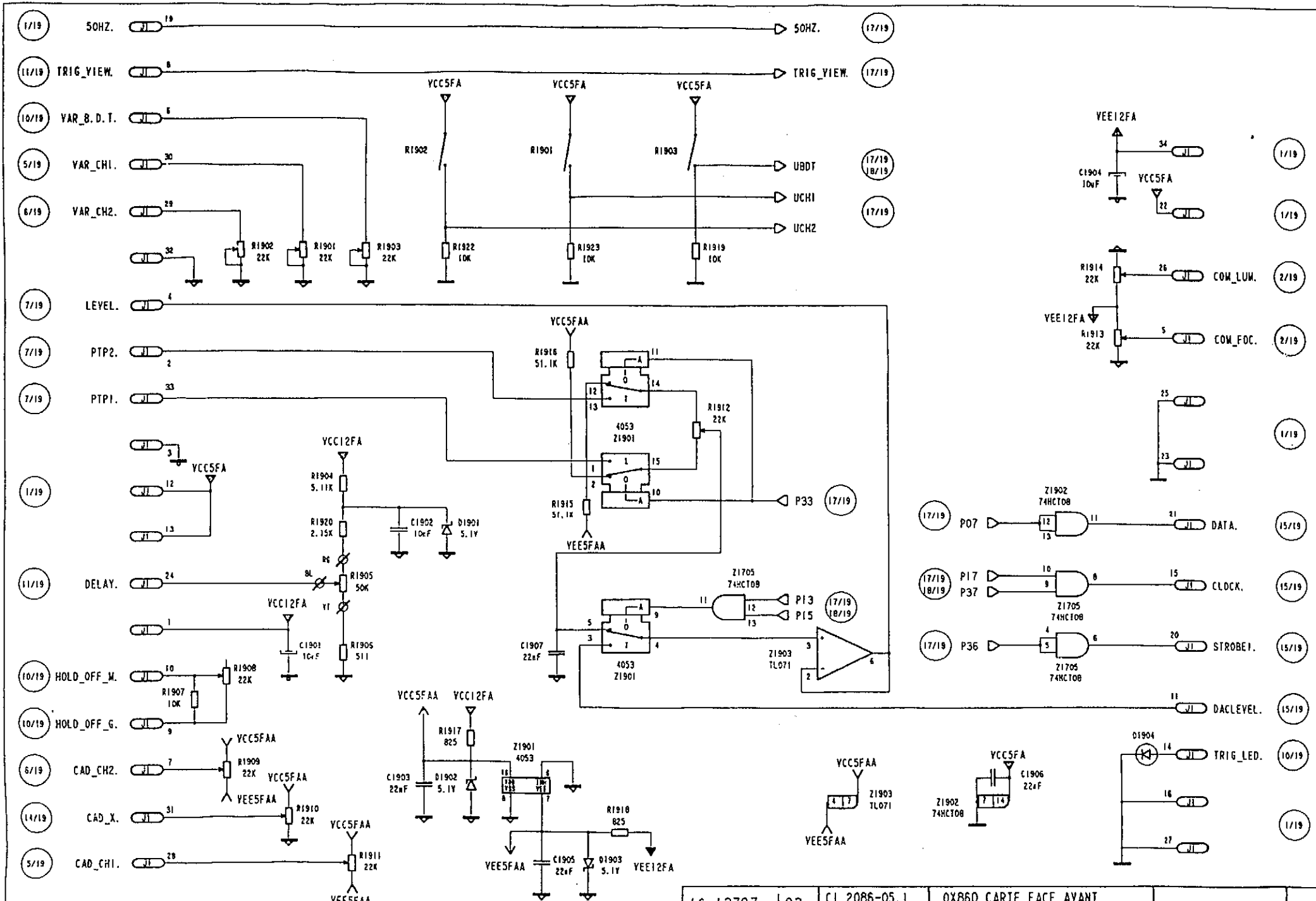

P16
UCH1
P37
UCH2
UBDT
TRIG_VIEW.
VCC5FA
VEE12FA
VCC12FA
Z1701 80C52
Z1702 TL7705ACD
Y1701 11.0592MHZ
Z1703 9346
Z1704 TL431
Z1705 74HCT08
Z1706 74HCT03
Z1707 74HCT03
Z1708 74HCT03
Z1709 74HCT03
Z1902 74HCT08
S1725 ENCODEUR_6BITS CH2
S1726 ENCODEUR_6BITS CH1
S1727 ENCODEUR_6BITS B&T
P20
P21
P22
P23
P24
P25
P26
P27
P33
P35
P36
P37
RXD.
TXD.
50HZ.
0,5V
P06
P07
P10
P11
P12
P13
P14
P15
P16
P17
TRACE_ROTATION.
IC 13725
03
CI 2086-05.1
HD 0188-00
0X860 CARTE FACE AVANT
(0X8620/27) MICRO-P.
DATE 8.1.1996
17/19



IC 13726	03	CI 2086-05.1	0X860 CARTE FACE AVANT		18/19
NUMERO	VERSION	HD 0188-00	(0X8620/27) MATRICE	DATE 8.1.1996	Fig


50HZ.
TRIG_VIEW.
VAR_B.D.T.
VAR_CH1.
VAR_CH2.
LEVEL.
PTP2.
PTP1.
DELAY.
HOLD_OFF_M.
HOLD_OFF_G.
CAD_CH2.
CAD_X.
CAD_CH1.
UBDT
UCH1
UCH2
P33
P07
P17
P37
P36
DATA.
CLOCK.
STROBE1.
DACLEVEL.
TRIG_LED.
COM_LUM.
COM_FOC.
VCC5FA
VCC5FAA
VCC12FA
VEE5FAA
VEE12FA
4053
Z1901
Z1705
74HCT08
Z1903
TL071
IC 13727
03
CI 2086-05.1
0X860 CARTE FACE AVANT
(0X8620/27) POT.
8.1.1996
19/19