MOTOROLA

MEDIUM-POWER
MRTL
INTEGRATED CIRCUITS
MC900/MC800 SERIES

MOTOROLA

MEDIUM-POWER MRTL INTEGRATED CIRCUITS

INDEX

DEVICE SPECIFICATIONS

MOTOROLA

FUNCTIONS AND CHARACTERISTICS

V_{CC} = 3.0 V ±10%, T_A = 25°C

Function	Type ① -55 to +125°C	0 to +100°C	Case	Output Loading Factor each output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
GATES						
3-Input NOR Gate	MC903	MC803	601, 606	5	12	19/5.0 ②
4-Input NOR Gate	MC907	MC807	601, 606	5	12	19/5.0 ②
Dual 2-Input NOR Gate	MC914	MC814	601, 606	5	12	38/10 ②
Dual 3-Input NOR Gate	MC915	MC815	603, 606	5	12	38/10 ②
Quad 2-Input NOR Gate	MC924	MC824	607	5	12	76/20 ②
Dual 4-Input NOR Gate	MC925	MC825	607	5	12	38/10 ②
5-Input NOR Gate	MC929	MC829	601, 606	5	12	19/5.0 ②
Quad Exclusive OR Gate	MC971	MC871	607	5	12	72
Triple 3-Input NOR Gate	MC992	MC892	607	5	12	57/15 ②
BUFFERS						
Buffer	MC900	MC800	601, 606	25	20	16/45 ②
Dual 3-Input Buffer, non inverting	MC988	MC888	607	25	24	128/42 ②
Dual Buffer	MC999	MC899	603, 606	25	20	32/90 ②
FLIP-FLOPS						
R-S Flip-Flop	MC902	MC802	601	4	14	22
J-K Flip-Flop	MC916	MC816	601, 606	3	30	62/54 ③
J-K Flip-Flop	MC926	MC826	603, 606	5	35	130/65 ③
J-K Flip-Flop	MC974	MC874	601	5	35	130/65 ③
Dual J-K Flip-Flop	MC990	MC890	607	3	35	124/108 ③
Dual J-K Flip-Flop	MC991	MC891	607	5	40	155/130 ③
HALF-SHIFT REGISTERS						
Half-Shift Register	MC905	MC805	601, 606	4	22	53
Half-Shift Register (w/o Inverter)	MC906	MC806	601, 606	4	22	36
Dual Half-Shift Register	MC983	MC883	607	4	22	110
Dual Half-Shift Register w/Inverter	MC984	MC884	607	4	22	75
ADDERS and SUBTRACTORS						
Half Adder	MC904	MC804	601, 606	5	14	45
Dual Half Adder	MC975	MC875	607	5	20	90
Dual Full Adder	MC996	MC896	607	5	60	190
Dual Full Subtractor	MC997	MC897	607	5	60	190
COUNTER ADAPTERS						
Counter Adapter	MC901	MC801	601	5	22	55
INVERTERS						
Quad Inverter	MC927	MC827	603, 606	5	12	76/20 ②
Hex Inverter	MC989	MC889	607	5	12	76/20 ②
EXPANDERS						
Quad 2-Input Expander	MC985	MC885	607	—	12	17/— ②
Dual 4-Input Expander	MC986	MC886	607	—	12	17/— ②
Hex Expander	MC9919	MC9819	607	—	12	13/— ②

① G Suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC900G = Metal Can, MC900F = Flat Package.
② Inputs High/Inputs Low
③ Only Clock Input High/Inputs Low

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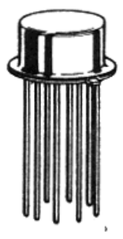
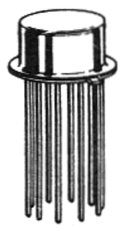
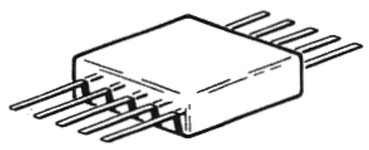
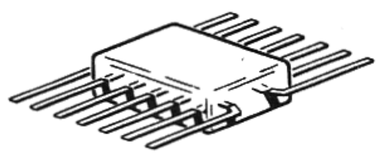
 **G SUFFIX** METAL PACKAGE CASE 601 TO-99	 **G SUFFIX** METAL PACKAGE CASE 603 TO-100	 **F SUFFIX** CERAMIC PACKAGE CASE 606 TO-91	 **F SUFFIX** CERAMIC PACKAGE CASE 607 TO-86

MAXIMUM RATINGS
($T_A = 25°C$)

Rating	Symbol	Value	Unit
Input Voltage	—	±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 s)	—	+12	Vdc
Operating Temperature Range MC900 Series MC800 Series	T_A	-55 to +125 0 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CONDITION TOLERANCES

$V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

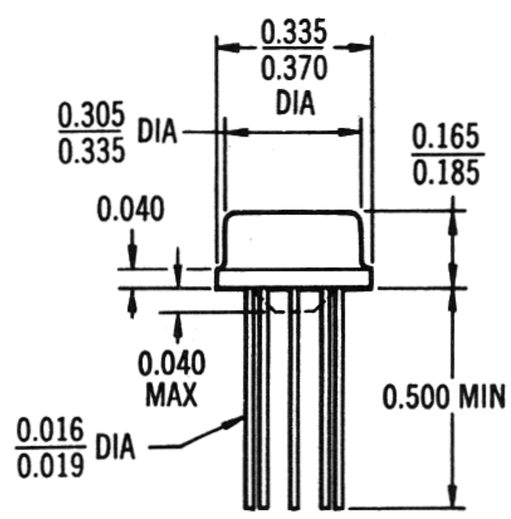
DEFINITIONS

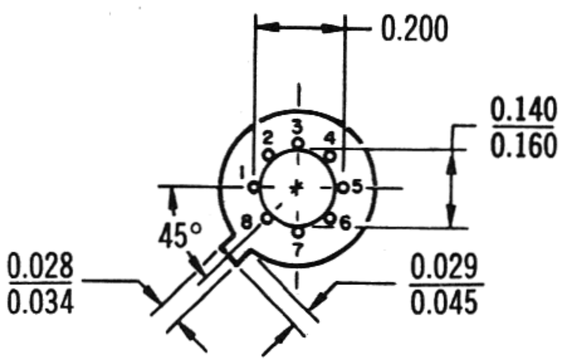
I_{A3}, I_{A4}, I_{A5}	Minimum available output current from a device with an output loading of 3, 4, or 5. Output voltage not to fall below the value of V_{in}.
I_{AB}	Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.
I_{CEX}	Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.
I_{in}	Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.
2 I_{in}, 3 I_{in}	Maximum input current drawn by one input of a device with 2 or 3 bases internally tied together.
V_{BOT}	A high-value voltage applied to an input of a device to insure saturation of the driven transistor.
V_{CC}	Supply voltage.
$V_{CE(sat)}$	Maximum saturation voltage with V_{BOT} applied to the input.
V_{in}	Minimum high-level voltage applied to the input of a device.
V_{off}	The maximum voltage which may be applied to an input terminal without turning the transistor on.
V_{on}	The minimum voltage which may be applied to an input terminal that will turn the transistor on.
V_{out}	The maximum output voltage with V_{on} applied to the input.
V_R	Value of external resistor connected to V_{CC} for test purposes. V_{RH} = highest node resistor value V_{RL} = lowest node resistor value
Release Time	The time that the J or K input data must be held after the negative-going clock input transition in order to propagate correct data.
Set-up Time	The time that the J or K input data must be present prior to the negative-going clock input transition in order to propagate correct data.

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- A gate output connected in parallel with another output reduces the drive capability by ½ load. (Paralleling gate circuits requires a V_{CC} connection to only one of the gates.)
- Any number of gates may be paralleled if the input loading is increased by ¼ load, if only one gate is connected to V_{CC}.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by 2 loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused inputs should be returned to ground.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled where the input loading factor is increased by 2.33.

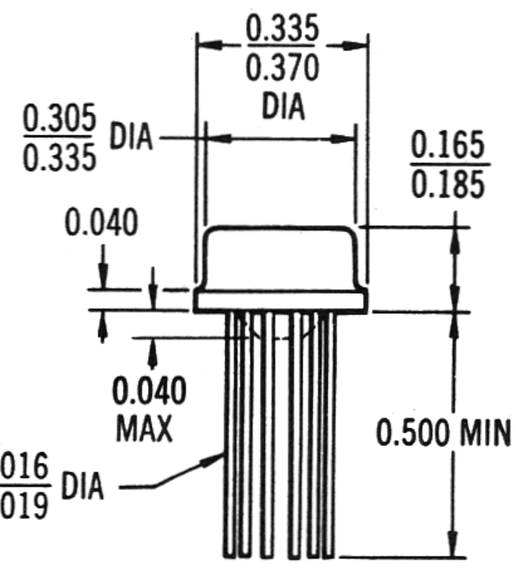
OUTLINE DIMENSIONS

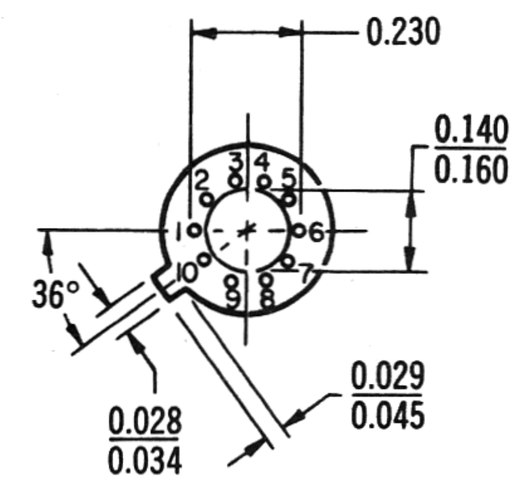




Pin 4 connected to case.

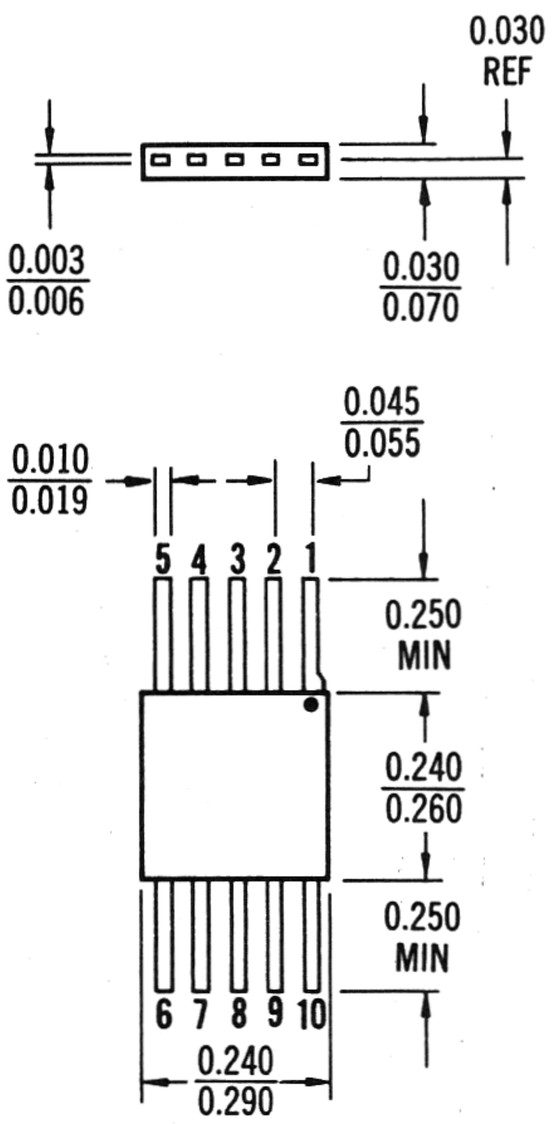
G SUFFIX
METAL PACKAGE
CASE 601
TO-99





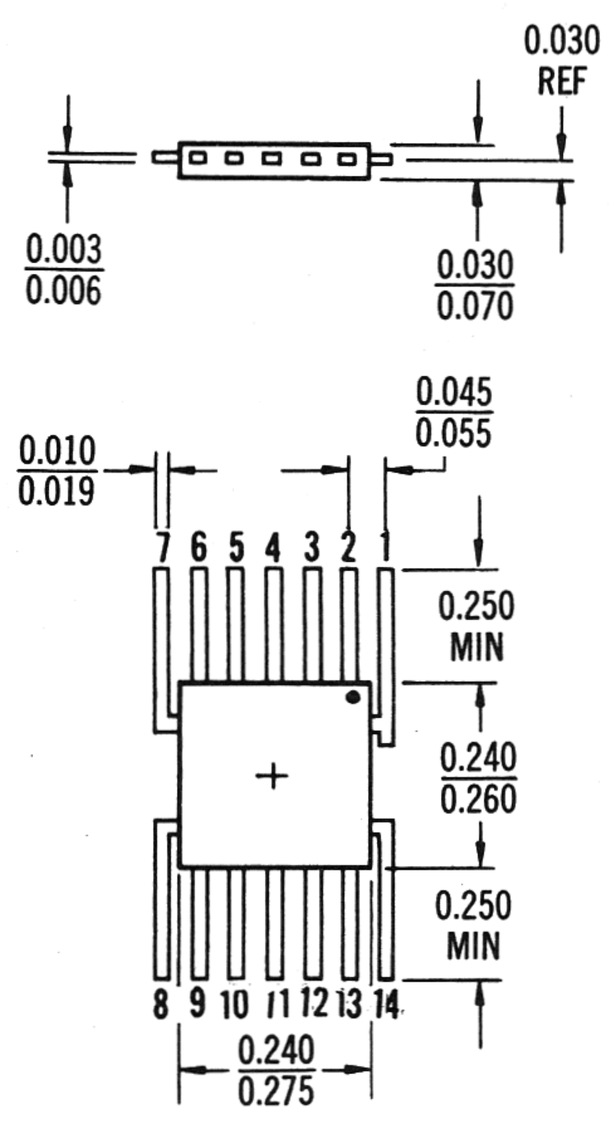
Pin 5 connected to case.

G SUFFIX
METAL PACKAGE
CASE 603
TO-100



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

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LOADING DIAGRAMS

MRTL MC900/800 series

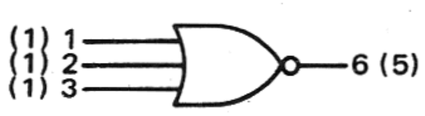
MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these two pages describe the MC900/MC800 MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

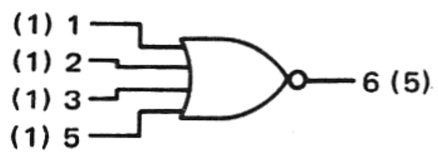
MC903G • MC803G
3-Input Gate



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

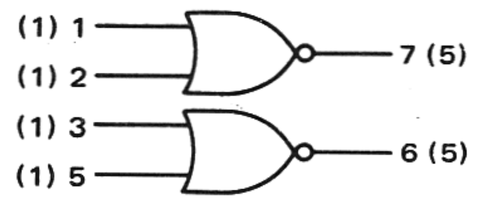
MC907G • MC807G
4-Input Gate



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

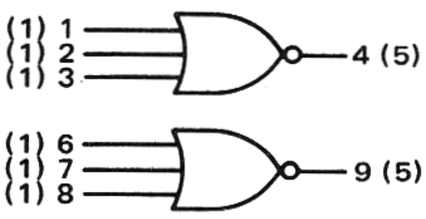
MC914G • MC814G
Dual 2-Input Gate



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

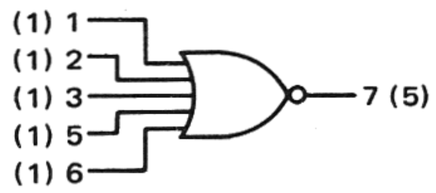
MC915G • MC815G
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

MC929G • MC829G
5-Input Gate

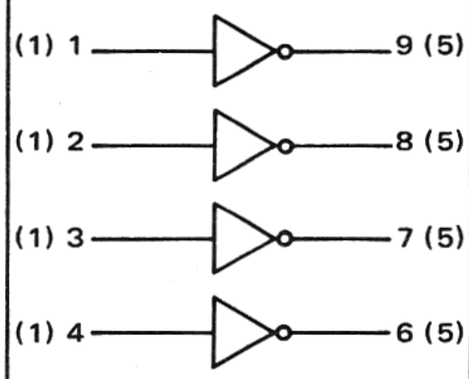


$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

INVERTERS

MC927G • MC827G
Quad Inverter

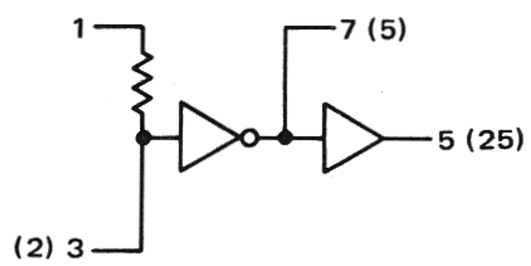


$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

BUFFERS

MC900G • MC800G
Buffer

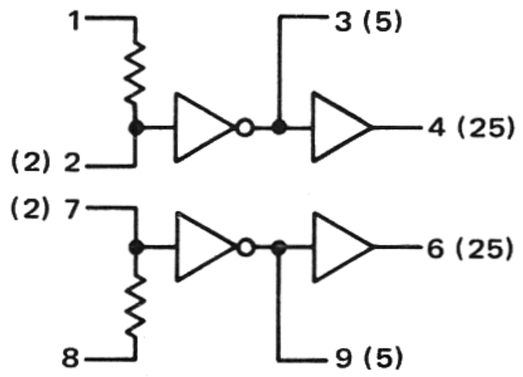


$7 = \overline{3}$

$5 = \overline{3}$

t_{pd} = 20 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999G • MC899G
Dual Buffer



$3 = \overline{2}$

$4 = \overline{2}$

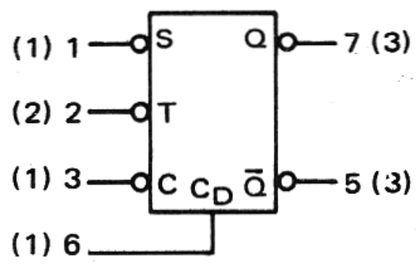
t_{pd} = 20 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

MOTOROLA

MRTL DEVICES AVAILABLE IN METAL CANS (continued)

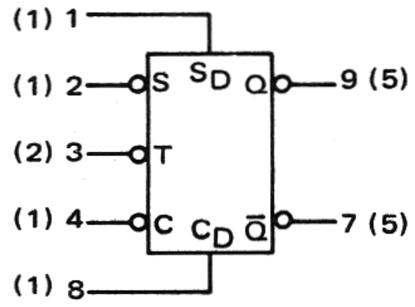
FLIP-FLOPS

MC916G • MC816G
J-K Flip-Flop



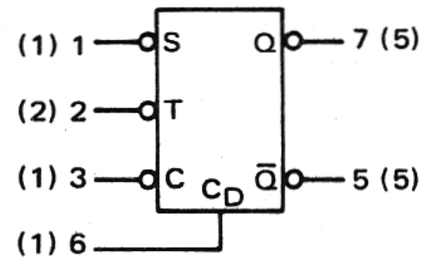
t_{pd} = 30 ns
P_D = 62 mW (Only Clock Input High)
54 mW (Inputs Low)

MC926G • MC826G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

MC974G • MC874G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC926 and MC826 only

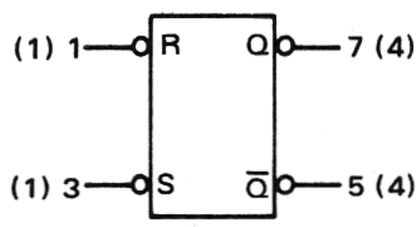
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC902G • MC802G
R-S Flip-Flop

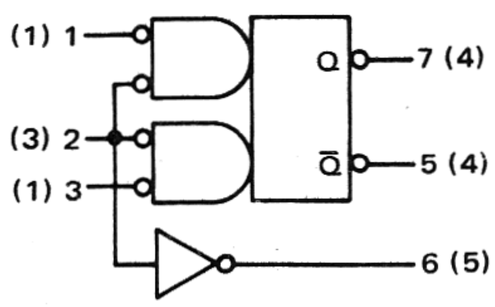


t_{pd} = 14 ns
P_D = 22 mW

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	0

HALF-SHIFT REGISTERS

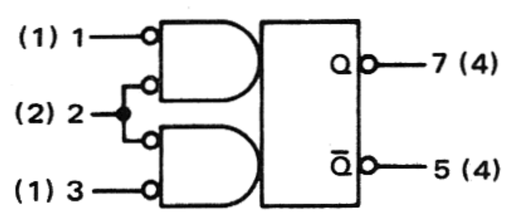
MC905G • MC805G
Half-Shift Register



t_{pd} = 22 ns
P_D = 53 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$
$6 = \overline{2}$

MC906G • MC806G
Half-Shift Register
(Without Inverter)

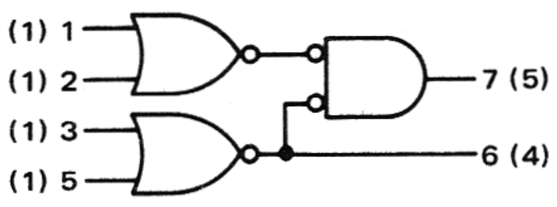


t_{pd} = 22 ns
P_D = 36 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$

HALF ADDERS

MC904G • MC804G
Half Adder

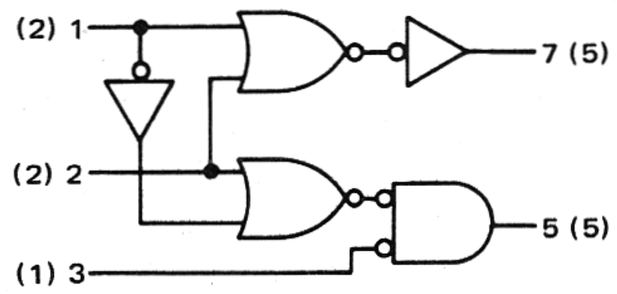


$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{3 + 5}$
t_{pd} = 14
P_D = 45

IF: $3 = \overline{1}$, & $5 = \overline{2}$
THEN: $6 = 1 \cdot 2$
$7 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

COUNTER ADAPTERS

MC901G • MC801G
Counter Adapter



t_{pd} = 22 ns
P_D = 55 mW

$7 = 1 + 2$
$5 = (\overline{1} + 2)\,\overline{3}$

MOTOROLA

LOADING DIAGRAMS

MRTL MC900/800 series

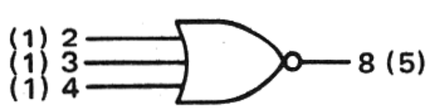
MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams on these four pages describe the MC900/MC800 MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability — fan-out — (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of −55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

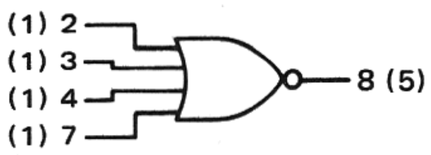
MC903F • MC803F
3-Input Gate



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

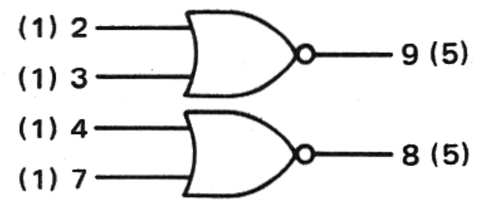
MC907F • MC807F
4-Input Gate



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

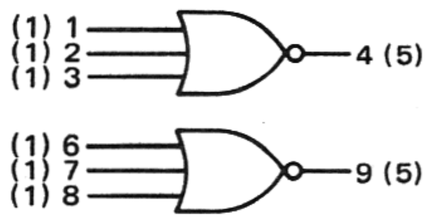
MC914F • MC814F
Dual 2-Input Gate



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

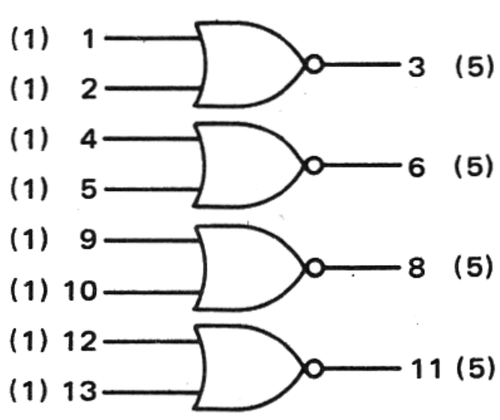
MC915F • MC815F
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

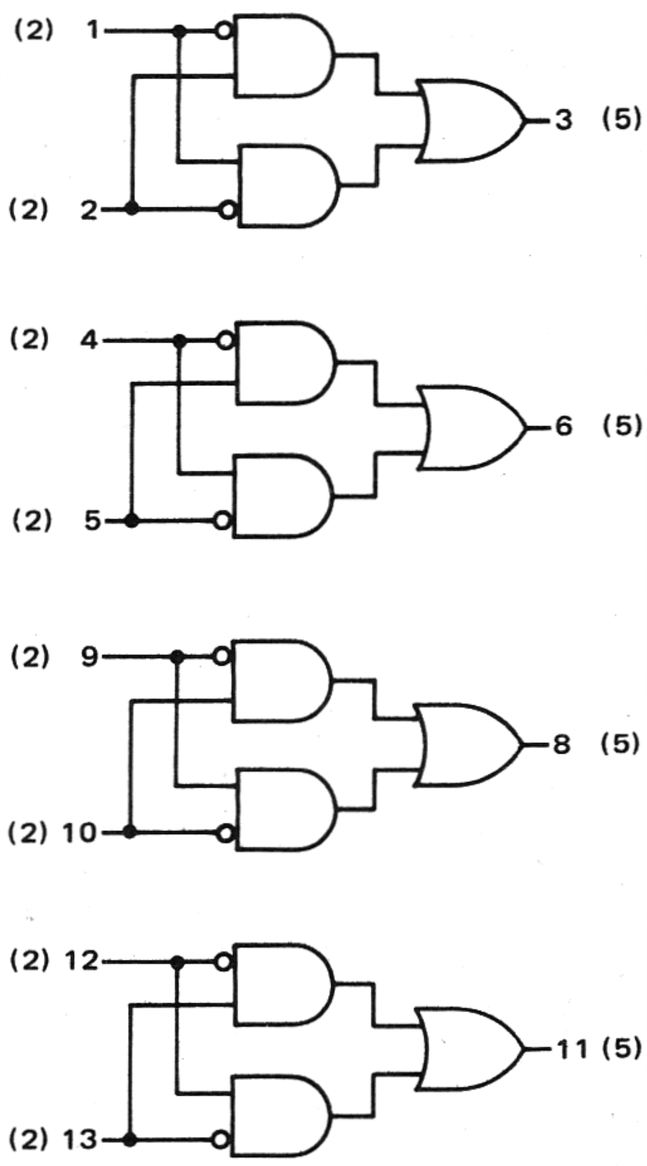
MC924F • MC824F
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

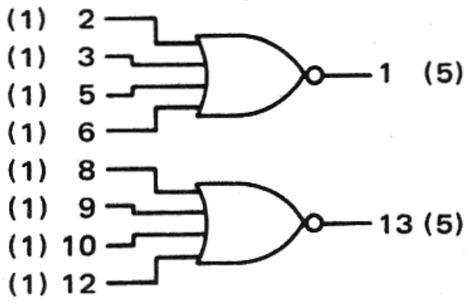
MC971F • MC871F
Quad Exclusive "OR" Gate



$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 72 mW

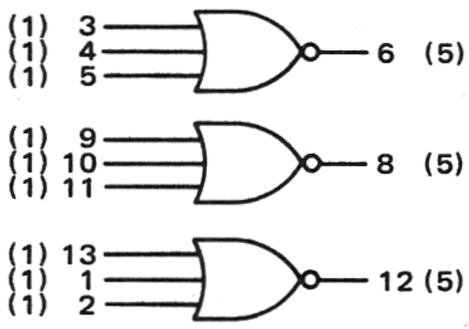
MC925F • MC825F
Dual 4-Input Gate



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

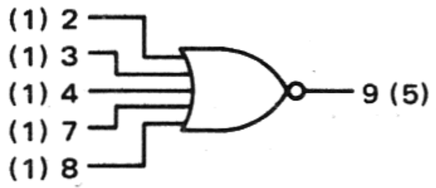
MC992F • MC892F
Triple 3-Input Gate



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 57 mW (Input High)
15 mW (Inputs Low)

MC929F • MC829F
5-Input Gate



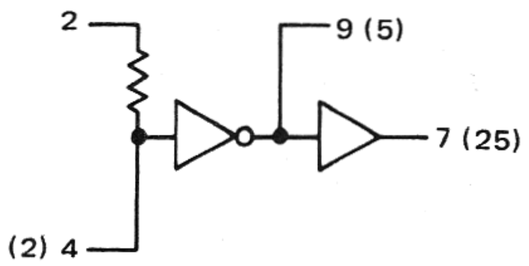
$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

MRTL DEVICES AVAILABLE IN FLAT PACKAGES (continued)

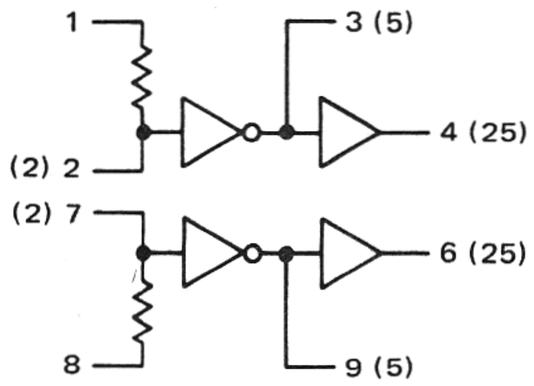
BUFFERS

MC900F • MC800F
Buffer



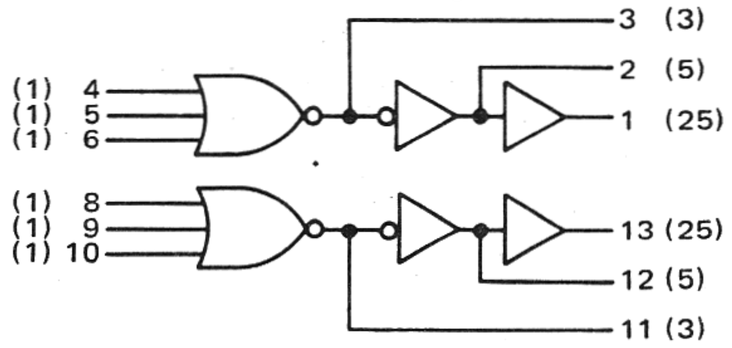
$9 = \overline{4}$
$7 = \overline{4}$
t_{pd} = 15 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999F • MC899F
Dual Buffer



$3 = \overline{2}$
$4 = \overline{2}$
t_{pd} = 15 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

MC988F • MC888F
Dual 3-Input Buffer
(Non-Inverting)



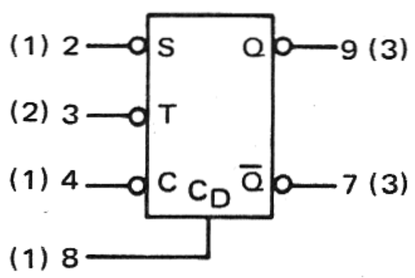
t_{pd} = 24 ns
P_D = 128 mW (Input High)
42 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$
$2 = 4 + 5 + 6$
$1 = 4 + 5 + 6$

Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

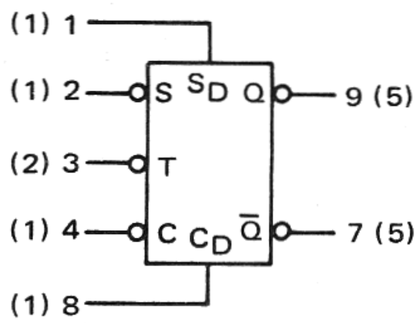
FLIP-FLOPS

MC916F • MC816F
J-K Flip-Flop



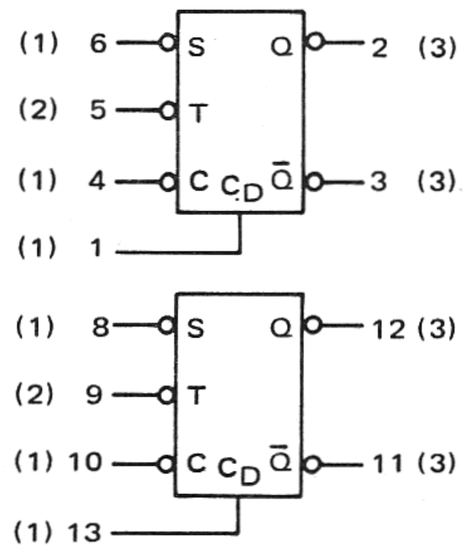
t_{pd} = 30 ns
P_D = 62 mW (Only Clock Inputs High)
54 mW (Inputs Low)

MC926F • MC826F
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Inputs High)
65 mW (inputs Low)

MC990F • MC890F
Dual J-K Flip-Flop



t_{pd} = 35 ns
P_D = 124 mW (Only Clock Inputs High)
108 Mw (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

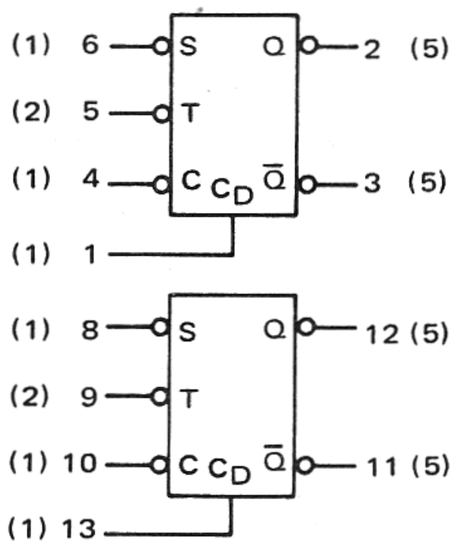
CLOCKED INPUT OPERATION ③
all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

J-K FLIP-FLOP TRUTH TABLES

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC991F • MC891F
Dual J-K Flip-Flop

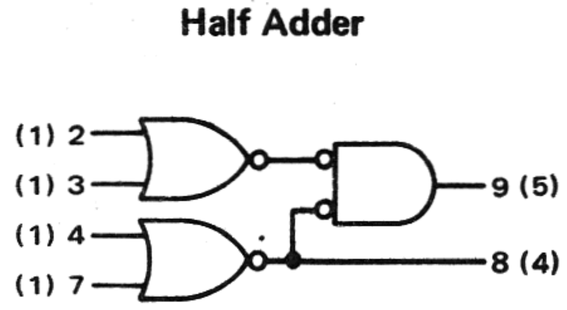


t_{pd} = 40 ns
P_D = 155 mW (Only Clock Input High)
130 mW (Inputs Low)

MRTL DEVICES AVAILABLE IN FLAT PACKAGES (continued)

HALF ADDERS

MC904F • MC804F
Half Adder



$9 = (2 + 3)\ (4 + 7)$

$8 = \overline{4 + 7}$

t_{pd} = 14 ns

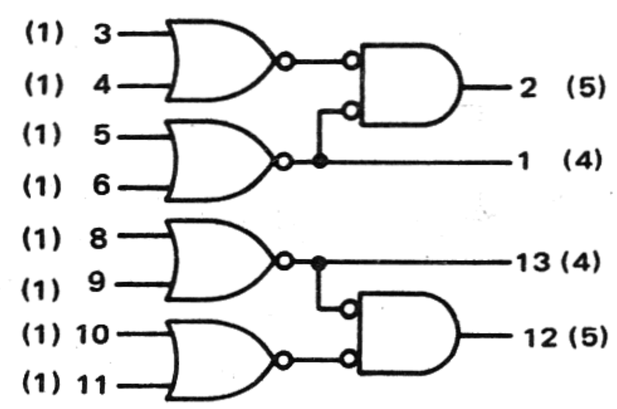
P_D = 45 mW

IF: $4 = \overline{2}$, & $7 = \overline{3}$

THEN: $8 = 2 \cdot 3$

$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

MC975F • MC875F
Dual Half Adder



t_{pd} = 20 ns

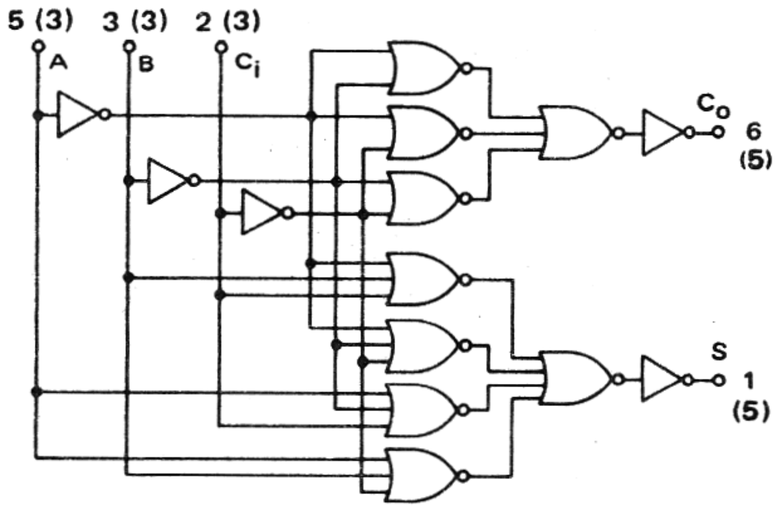
P_D = 120 mW

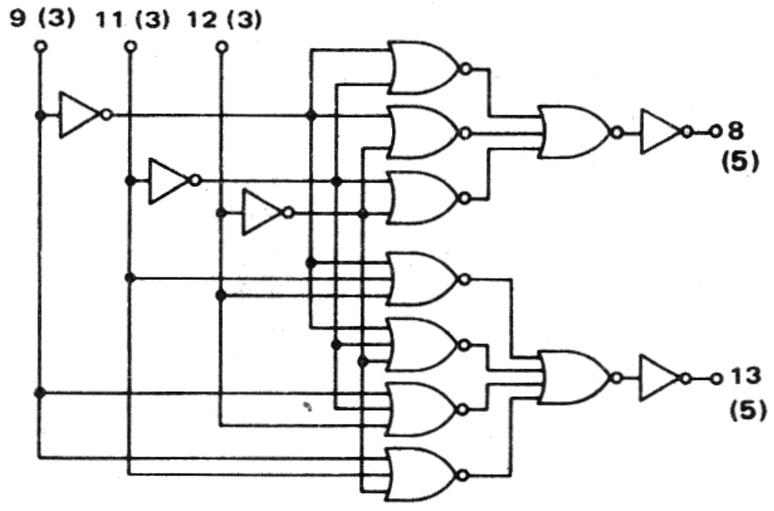
$2 = (3 + 4)\ (5 + 6)$

$1 = \overline{5 + 6}$

FULL ADDER

MC996F • MC896F
Dual Full Adder





$C_o = ABC_i + AB\overline{C}_i + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + A\overline{B}\overline{C}_i + \overline{A}\overline{B}C_i + \overline{A}B\overline{C}_i$

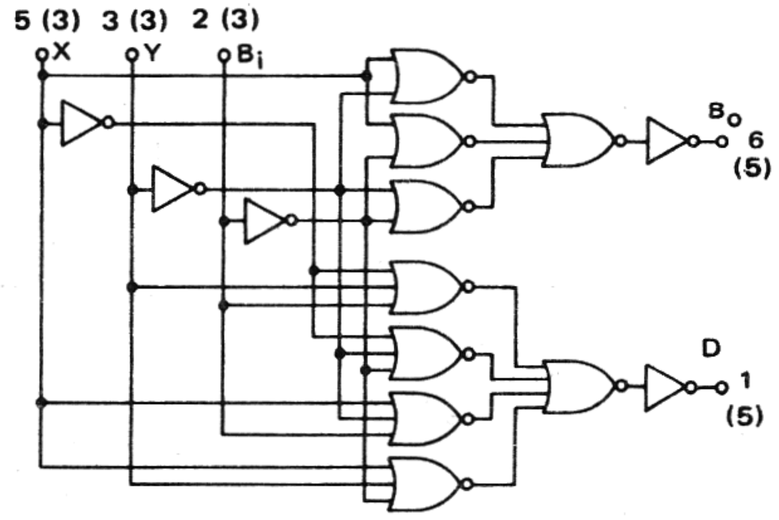
t_{pd} = 60 ns

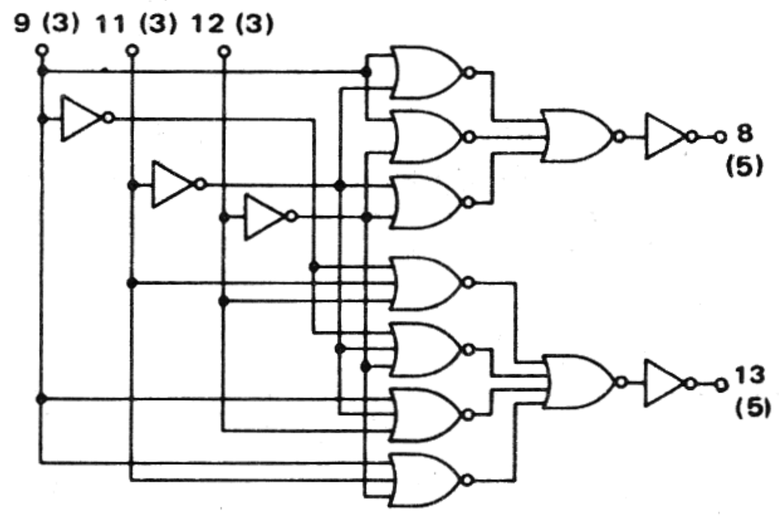
P_D = 190 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC997F • MC897F
Dual Full Subtractor





$D = YXB_i + Y\overline{X}\overline{B}_i + \overline{Y}X\overline{B}_i + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B}_i + Y\overline{X}B_i + YXB_i$

t_{pd} = 60 ns

P_D = 190 mW

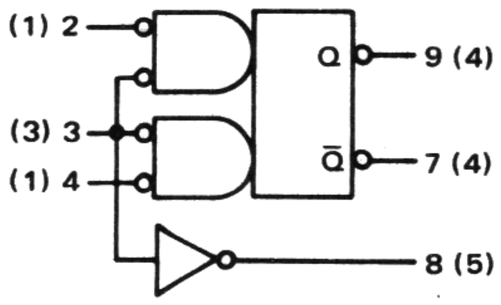
TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

MOTOROLA

MRTL DEVICES AVAILABLE IN FLAT PACKAGES (continued)

HALF-SHIFT REGISTERS

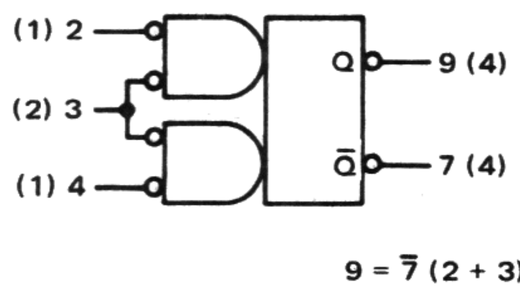
MC905F • MC805F
Half-Shift Register



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$
$8 = \overline{3}$

t_{pd} = 22 ns
P_D = 53 mW

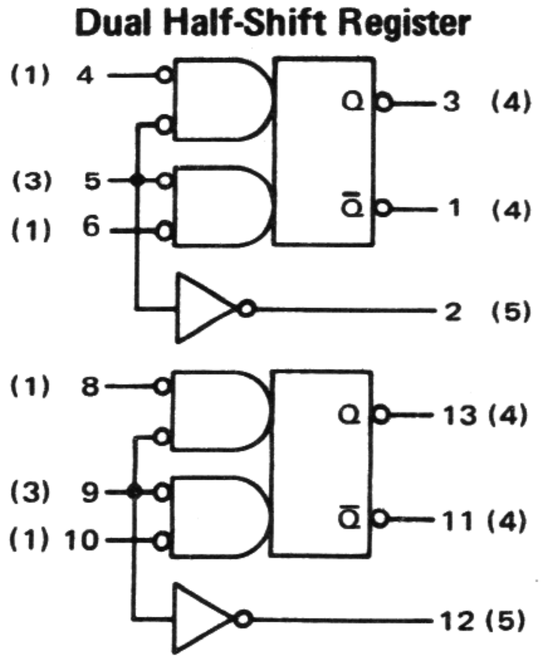
MC906F • MC806F
Half-Shift Register
(Without Inverter)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$

t_{pd} = 22 ns
P_D = 36 mW

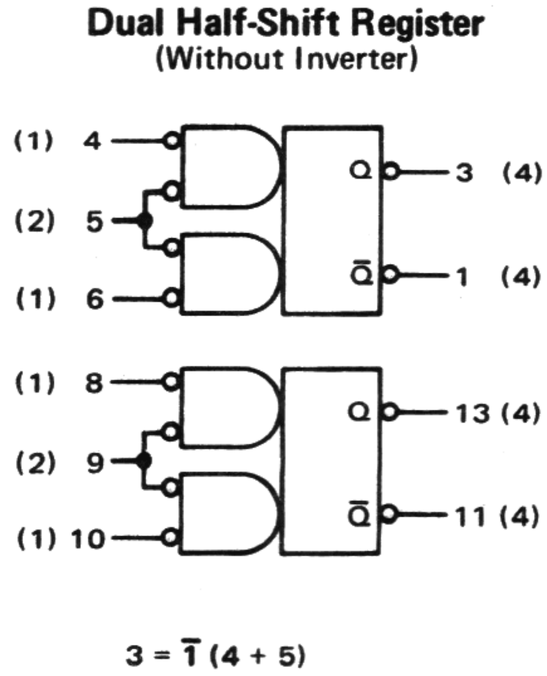
MC983F • MC883F
Dual Half-Shift Register



$1 = \overline{3}\ (6 + 5)$
$3 = \overline{1}\ (5 + 4)$
$2 = \overline{5}$

t_{pd} = 22 ns
P_D = 110 mW

MC984F • MC884F
Dual Half-Shift Register
(Without Inverter)

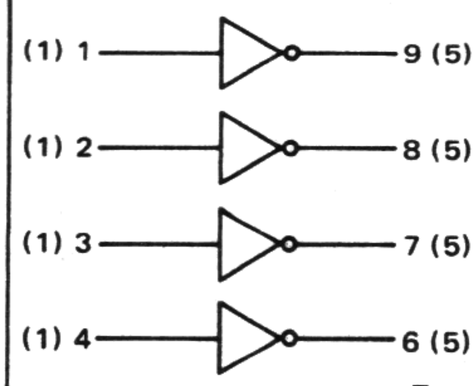


$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 75 mW

INVERTERS

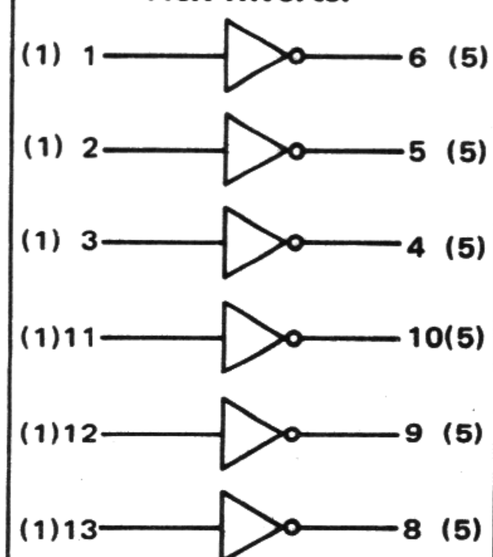
MC927F • MC827F
Quad Inverter



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

MC989F • MC889F
Hex Inverter

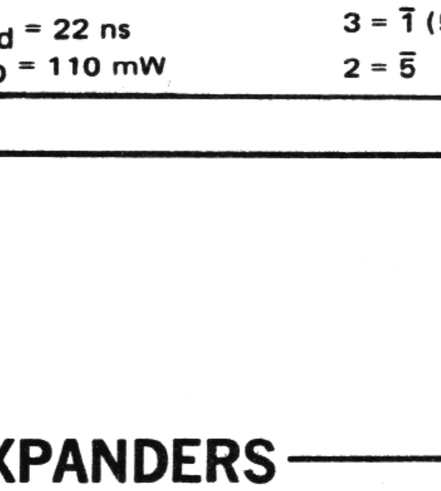


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

EXPANDERS

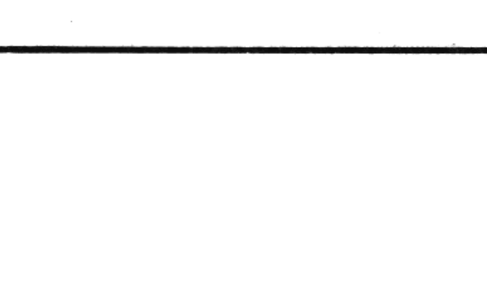
MC985F • MC885F
Quad 2-Input Expander



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 17 mW (input High)
Negligible (Inputs Low)

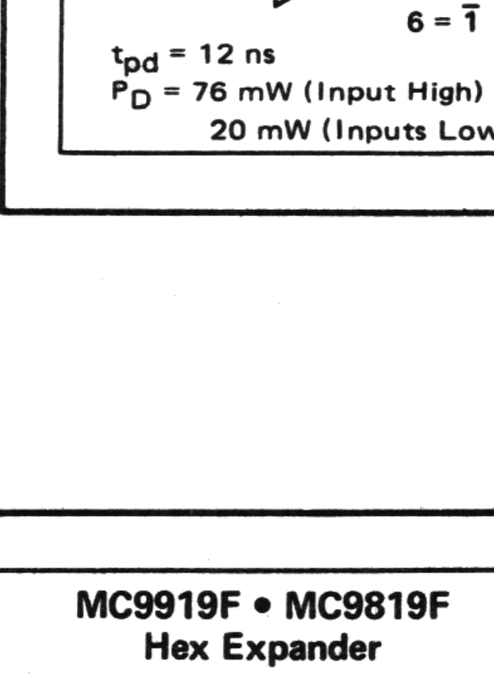
MC986F • MC886F
Dual 4-Input Expander



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 17 mW (Input High)
Negligible (Inputs Low)

MC9919F • MC9819F
Hex Expander



$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)