National Semiconductor

MOS ROMs

MM5213 2048-Bit (256 × 8 or 512 × 4) ROM

General Description

The MM5213 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

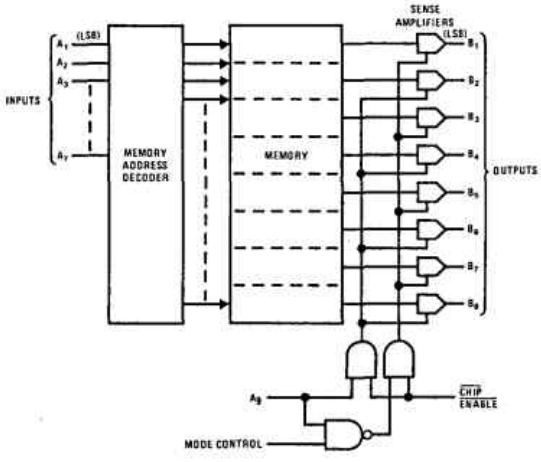
Features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 600 ns typ
- Pin compatible with MM5203 PROM
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control
- TRI-STATE output

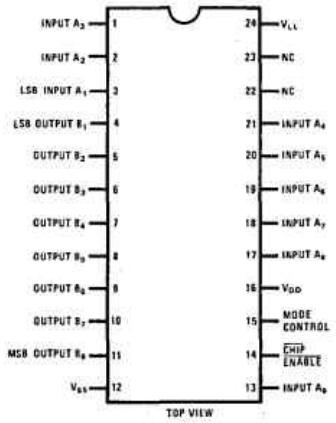
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5213J
See NS Package J24A

Order Number MM5213N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{LL} Supply Voltage	V_{SS} − 20V
V_{DD} Supply Voltage	V_{SS} − 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.3)\ V$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature	0°C to +70°C

Electrical Characteristics POSITIVE LOGIC (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Capability					
Logical "1"	V_{OUT} = 2.4V	200			μA
Logical "0"	V_{OUT} = 0.4V	−1.6			mA
Input Voltage Levels					
Logical "0"				V_{SS} − 4.0	V
Logical "1"		V_{SS} − 2.0			V
Power Supply Current	T_A = 25°C				
I_{SS} (Note 2)	V_{SS} = +5V		20	40	mA
	$V_{LL} = V_{DD}$ = −12V				
Input Leakage	V_{IN} = −12V			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5		pF
Address Time					
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V		600	850	ns
	$V_{GG} = V_{DD}$ = −12.0V				
Output AND Connections (Note 4)				10	

Note 1: These specifications apply for V_{SS} = +5.0V ±5%, V_{LL} = −12V, T_A = −25°C to +70°C unless otherwise specified.

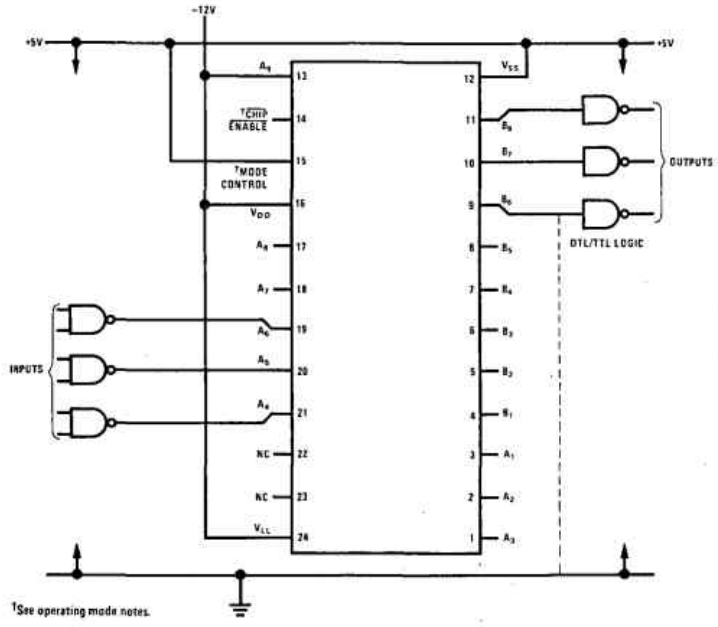
Note 2: Outputs open.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate.

Note 4: The address time in the TTL load configuration follows the equation: T_{ACCESS} = The specified limit + (N − 1) (25) ns. Where N = Number of AND connections.

Note 5: Capacitances are measured on a lot sample basis only.

Typical Applications (Continued)



Operating Modes

256x8 ROM connection (shown)
Mode Control — Logic "1"
A_9 — Logic "0"

512x4 ROM connection
Mode Control — Logic "0"
A_9 — Logic "1" Enables the odd (B_1, B_3 . . . B_9) outputs
— Logic "0" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "0" is applied to the Chip Enable line.

Mode Control should be "hard wired" to V_{LL} (Logical "0") or V_{SS} (Logical "1").