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DATA SHEET

PCF29F64
8 K x 8-bit static CMOS EEPROM with PAGE-ERASE option

Preliminary specification
File under Integrated Circuits, IC10

January 1993

PHILIPS

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8 K x 8-bit static CMOS EEPROM with PAGE-ERASE option

PCF29F64

FEATURES

- Low Power CMOS
  - maximum active current 10 mA
  - maximum standby current 200 µA
- Access time 200 ns
- Fast Erase cycle time
  - 32-byte Erase operation (PAGE-Erase) 5 ms
  - 256-byte Erase operation (BLOCK-Erase) 5 ms
  - complete Memory Erase operation 5 ms
- Fast Write cycle time 2.5 ms
- $\overline{\text{Data}}$ Polling allows user to minimize Write cycle time
- Simple Write operation
  - single TTL-level $\overline{\text{WE}}$ signal
  - internally latched address and data
  - automatic Write timing
- Endurance 10 000; T_{amb} = 85 °C
- 10 years non-volatile data retention time.

GENERAL DESCRIPTION

The PCF29F64 is an 8 K x 8-bit floating gate electrically erasable programmable read only memory (EEPROM), fabricated in a 1.2 micron n-channel floating gate CMOS technology.

Power consumption is very low and reliability is high due to the full CMOS technology used, as that for the PCX8582 family.

Three different Erase-operation modes are offered by the PCF29F64:

- 32-byte Erase operation (PAGE)
- 256-byte Erase operation (BLOCK)
- Complete Memory Erase operation

A write operation is performed in approximately 2.5 ms, which allows the entire memory to be written in less than 21 s.

The PCF29F64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

Philips EPROMs and PAGE-EEPROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	–	5.5	V
I_{DDR}	supply current READ				
	CMOS inputs	–	–	5	mA
I_{DDW}	supply current WRITE/ERASE				
	CMOS inputs	–	–	10	mA
I_{DDO}	standby supply current				
	CMOS input level	–	–	200	µA
	TTL input level	–	–	2	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF29F64P	28	DIL	plastic	SOT117
PCF29F64T	28	SO28	plastic	SOT136

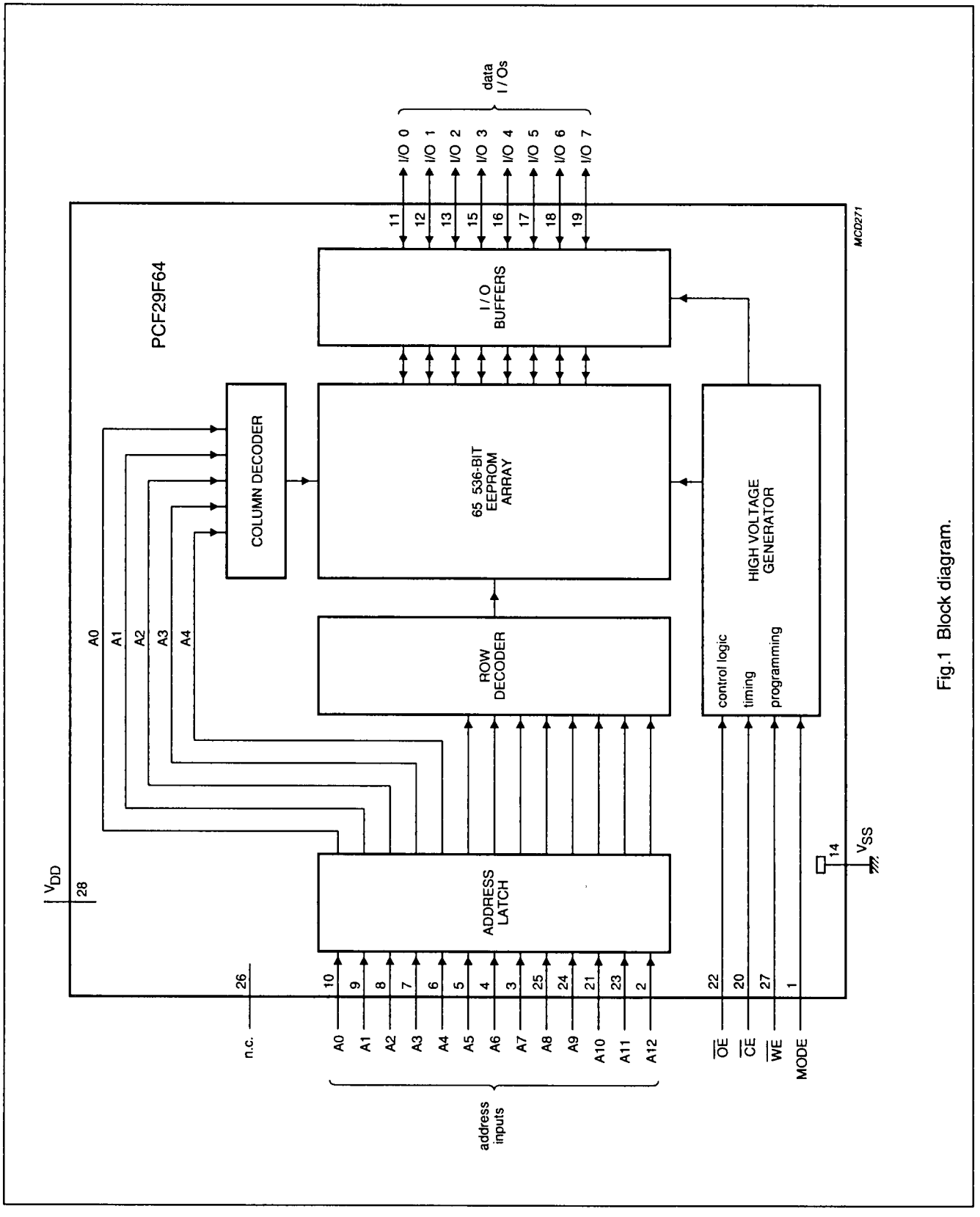


Fig.1 Block diagram.

8 K x 8-bit static CMOS EEPROM with PAGE-ERASE option

PCF29F64

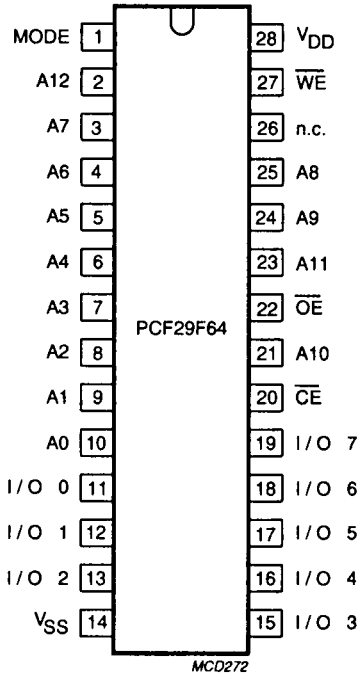


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
MODE	1	selection of Erase mode is achieved by a HIGH at this input, LOW selects the Write mode
A0 to A7 A8, A9 A10, A11, A12	10 to 3 25, 24 21, 23, 2	address inputs which select an 8-bit memory location during a read or write operation
I/O 0 to I/O 7	11 to 13, 15 to 19	data is written to or read from the PCF29F64 via the I/O pins
V_{SS}	14	negative supply voltage
$\overline{CE}$	20	Chip Enable input which must be LOW to enable all read/write operations, when HIGH power consumption is reduced
$\overline{OE}$	22	Output Enable input which controls the data output buffers and is used to initiate read operations
n.c.	26	not connected
$\overline{WE}$	27	Write Enable input which controls the writing of data to the PCF29F64
V_{DD}	28	positive supply voltage

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	V_{SS} −0.8	V_{DD} +0.8	V
I_I	current on any input pin		−	1	mA
I_O	output current		−	5	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	–	5.5	V
I_{DDR}	supply current READ	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}; outputs open; f = 5 MHz; other inputs = V_{IL} or V_{IH}				
	CMOS input level		–	–	5.0	mA
I_{DDW}	supply current ERASE/WRITE	see Figs 4 to 7				
	CMOS input level		–	–	10.0	mA
I_{DDO}	supply current STANDBY	$\overline{CE}$ = V_{IH}; $\overline{OE}$ = V_{IL}; all other pins = V_{IL} or V_{IH}				
	CMOS input level		–	–	200	µA
	TTL input level		–	–	2	mA
V_{IL}	LOW level input voltage					
	CMOS		V_{SS}−0.3	–	V_{SS}+0.3	V
	TTL		−1.0	–	0.8	V
V_{IH}	HIGH level input voltage					
	CMOS		V_{DD}−0.3	–	V_{DD}+0.3	V
	TTL		2.0	–	V_{DD}+1.0	V
V_{OL}	LOW level output voltage	I_{OL} = 2.1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −400 µA	2.4	–	–	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–	–	1	µA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}; $\overline{CE}$ = V_{IH}	–	–	1	µA
C_I	input capacitance	V_I = V_{SS}	–	–	tbf	pF
C_{VO}	input/output capacitance	V_{VO} = V_{SS}	–	–	tbf	pF
t_{PU}	power-up to operation time		–	5	–	ms

TIMING CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Read cycle				
t_{RC}	read cycle time	200	–	ns
t_{AA}	address access time	–	200	ns
t_{CE}	chip enable access time	–	200	ns
t_{OE}	output enable access time	–	100	ns
t_{LZ}	chip enable to output LOW Z	0	–	ns
t_{OLZ}	output enable to output LOW Z	0	–	ns
t_{HZ}	chip disable to output HIGH Z	0	50	ns
t_{OHZ}	output disable to output HIGH Z	0	50	ns
t_{OH}	output hold time from address change	10	–	ns
Erase and Write cycle				
t_{EC}	erase cycle time	4	6	ms
t_{WC}	write cycle time	2	3	ms
t_{AS}	address set-up time	10	–	ns
t_{AH}	address hold time	200	–	ns
t_{CS}	operation set-up time	0	–	ns
t_{CH}	operation hold time	0	–	ns
t_{CW}	chip enable pulse width	150	–	ns
t_{OES}	output enable HIGH set-up time	10	–	ns
t_{OEH}	output enable HIGH hold time	10	–	ns
t_{WP}	write enable pulse width	150	–	ns
t_{WPH}	write enable HIGH recovery time	50	–	ns
t_{DV}	data valid time	–	300	ns
t_{DS}	data set-up time	100	–	ns
t_{DH}	data hold time	20	–	ns

AC TEST CONDITIONS

Input pulse levels	0 to 3 V
Input rise and fall times	10 ns
Input and output timing levels	1.5 V
Output load	1 TTL gate and C_L = 100 pF

Table 1 Mode selection.

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O PIN	POWER
L	L	H	read	D OUT	active
L	H	L	erase (MODE input = HIGH)	–	active
L	H	L	write (MODE input = LOW)	D IN	active
H	X	X	standby and E/W inhibit	HIGH Z	standby
X	L	X	E/W inhibit	–	–
X	X	H	E/W inhibit	–	–

Table 2 Erase mode selection.

MODE/ADDRESS	A0 to A2	A3	A4	A5 to A7	A8 to A12
PAGE	X	0	0	valid	valid
BLOCK ERASE	X	0	1	X	valid (note 1)
BLOCK ERASE	X	1	0	X	valid (note 1)
FULL ERASE	X	1	1	X	X

Note to Table 2

1. If either A3 or A4 have a HIGH level, BLOCK ERASE mode is selected.

DEVICE OPERATIONS

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ set LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Erase

Erase operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ and MODE are HIGH. The PCF29F64 supports a $\overline{CE}$ and $\overline{WE}$ controlled cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, which ever occurs last.

An Erase operation, once initiated, will automatically continue to completion, typically within 5 ms.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The PCF29F64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2.5 ms.

$\overline{\text{Data}}$ Polling

The PCF29F64 features $\overline{\text{Data}}$ polling as a method to indicate to the host system that the byte write cycle has completed. $\overline{\text{Data}}$ polling allows a simple bit test operation to determine the status of the PCF29F64 eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O 7

(i.e. write data = 0XXX XXXX; read data = 1XXX XXXX)

Once the programming cycle is complete, I/O 7 will reflect true data.

ERASE-WRITE PROTECTION

There are three features that protect the non-volatile data from inadvertent Erase and Write operations.

- Noise protection; write pulse of less than 20 ns will not initiate a write cycle.
- V_{DD} sense; all functions are inhibited when V_{DD} is ≤ 3.5 V typically.
- E/W inhibit; holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent Erase and Write operations.

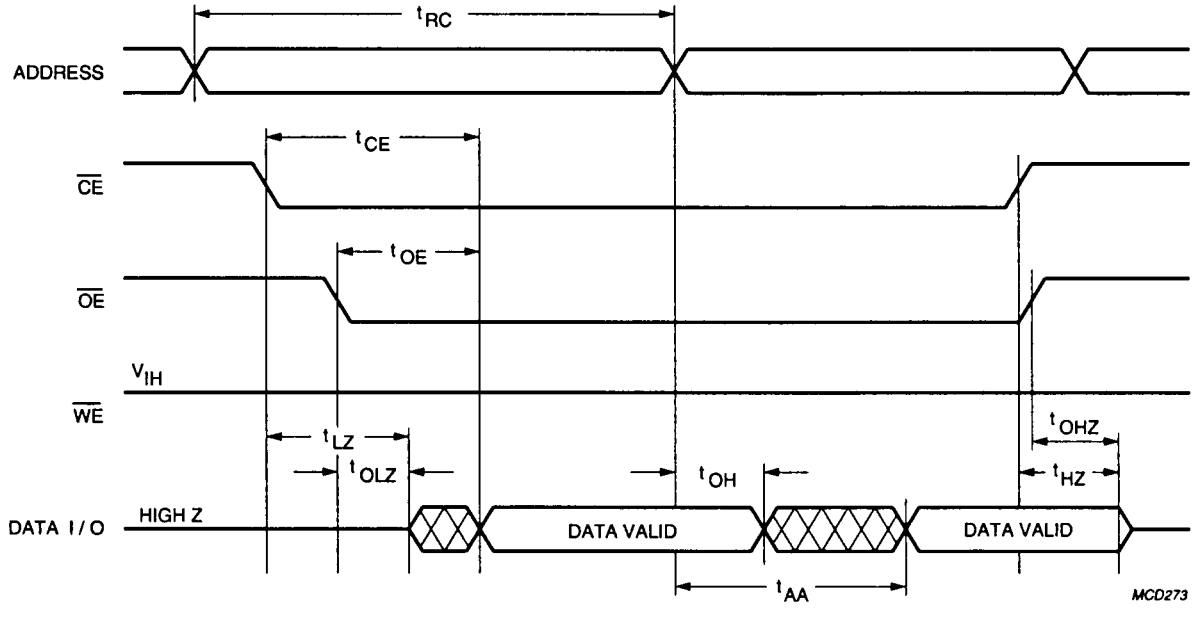


Fig.3 Timing diagram; Read cycle.

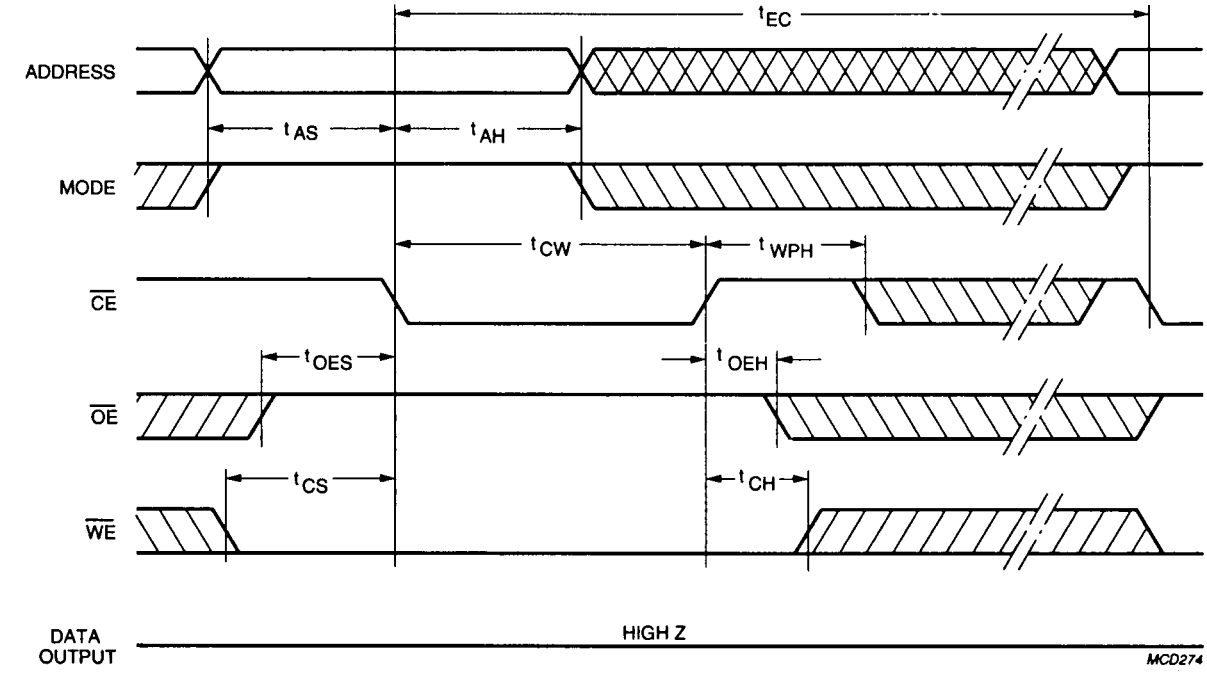


Fig.4 Timing diagram; $\overline{CE}$ controlled Erase cycle.

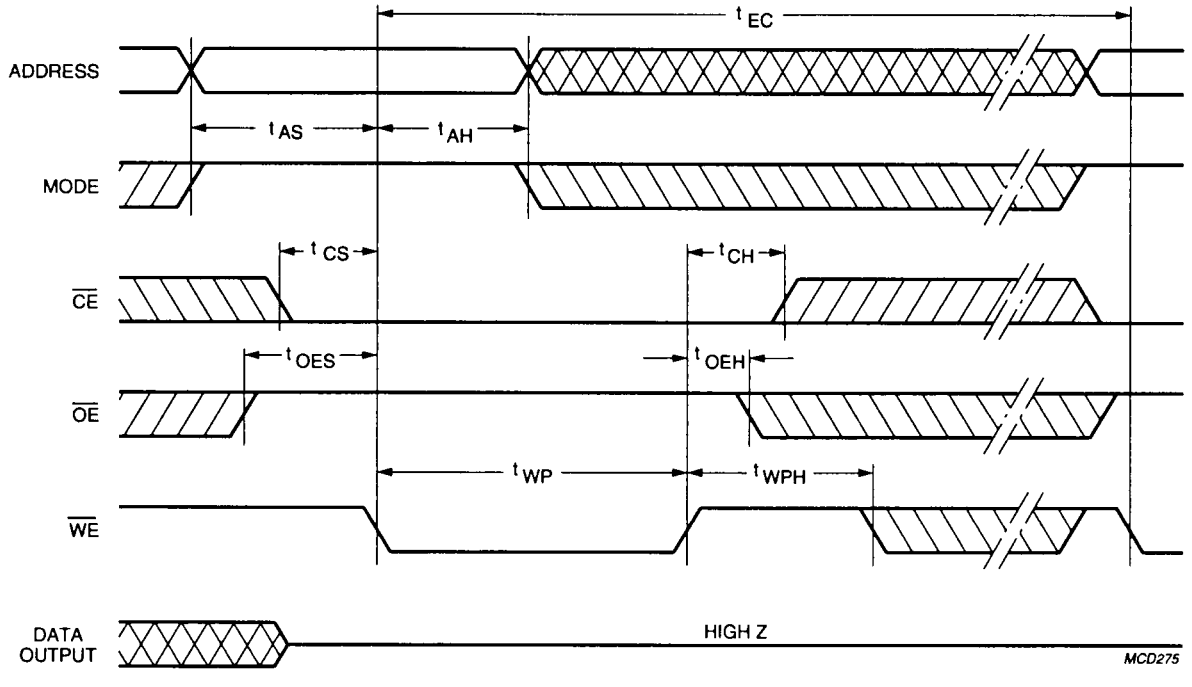


Fig.5 Timing diagram; $\overline{WE}$ controlled Erase cycle.

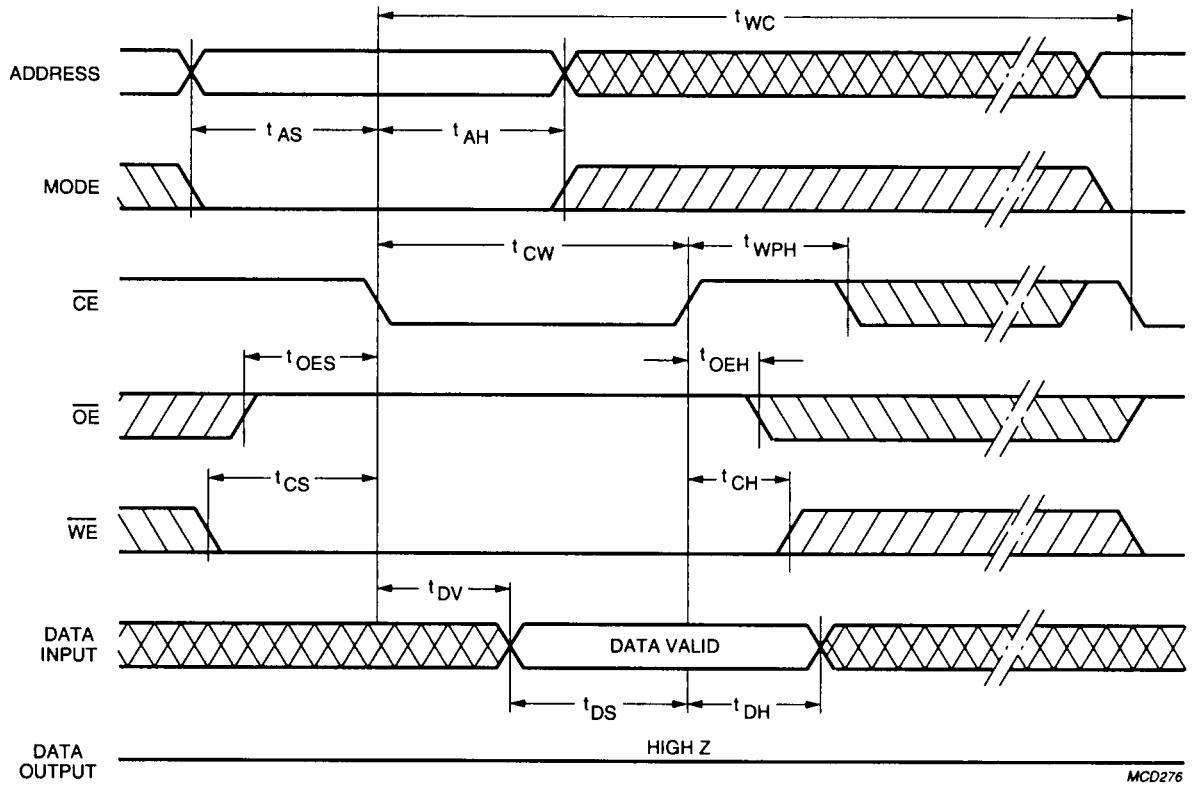


Fig.6 Timing diagram; $\overline{CE}$ controlled Write cycle.

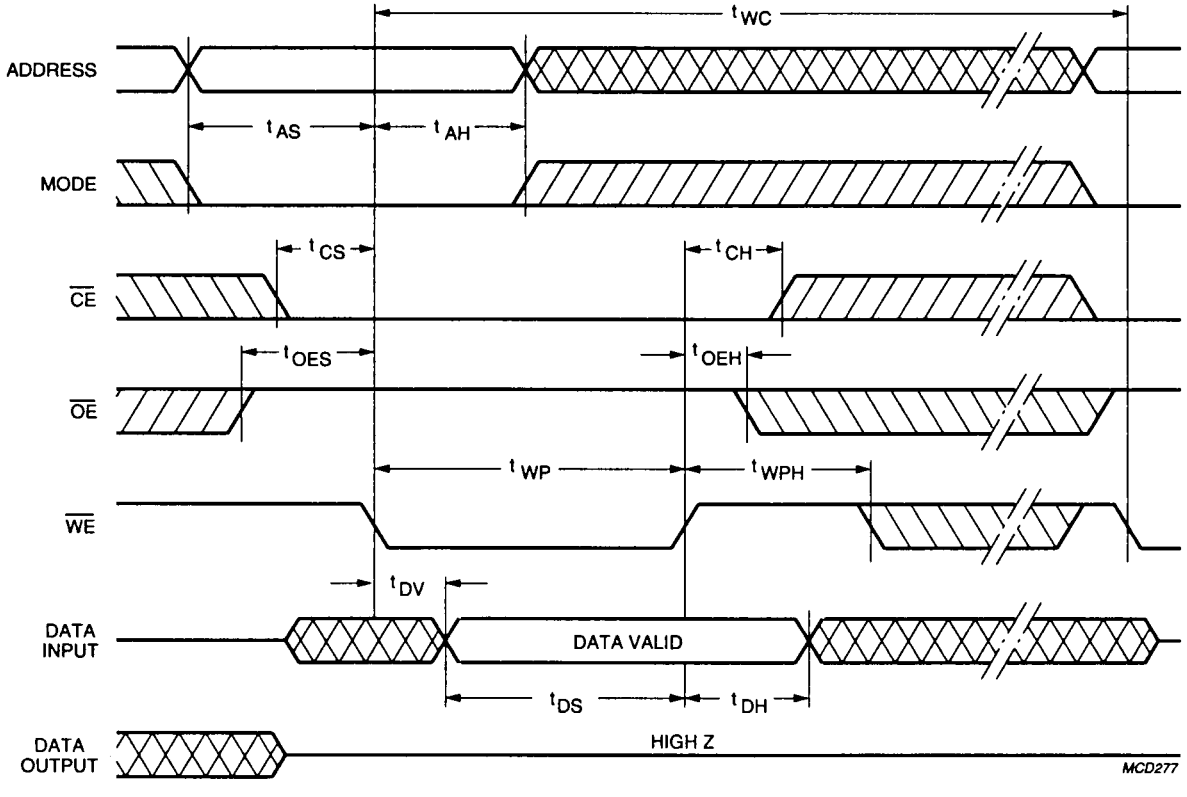


Fig.7 Timing diagram; $\overline{WE}$ controlled Write cycle.

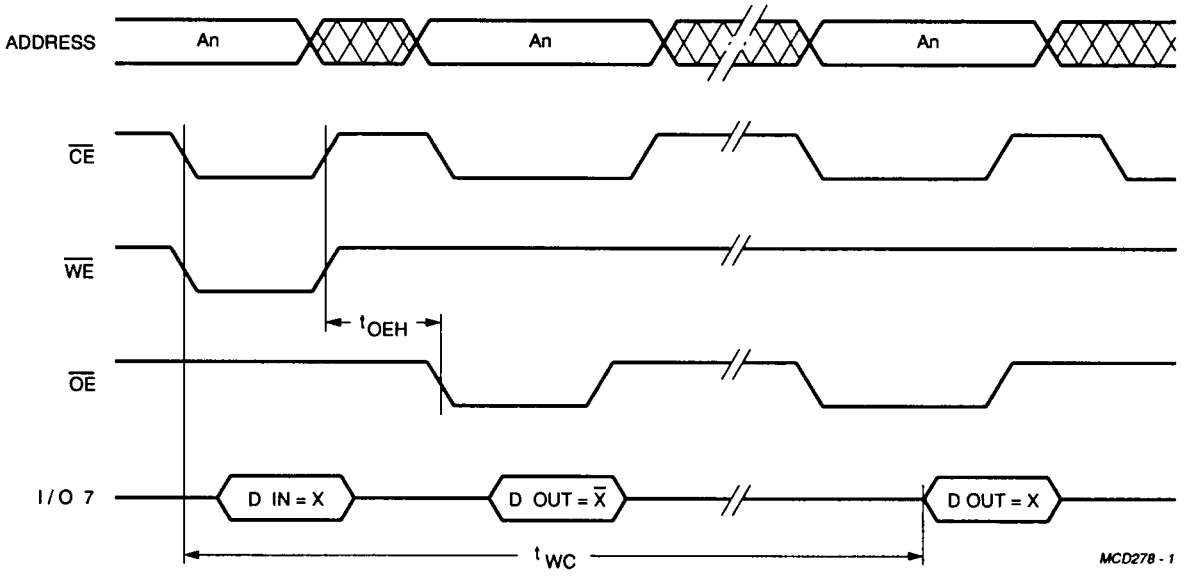


Fig.8 Timing diagram; $\overline{\text{Data}}$ polling.

APPLICATION INFORMATION

The use of Flash EEPROM (FEEPROM) facilitates opportunities to make embedded applications where new releases of firmware or modified parameter sets can be programmed by means of in-circuit programming.

Advantages of in-circuit programming over existing programming schemes are:

- No loss of time due to UV erasing
- No desoldering required. This is critical in applications with high component densities.
- No expensive and large sockets required. This becomes important when e.g. QFP packages are used.

The in-circuit programming of FEEPROM in an application can be initiated via e.g. a terminal or PC. In-circuit programming may also be controlled from a remote location via e.g. an RS232, RS485 or a telephone link. This makes the modification of firmware in applications that are installed in remote locations (e.g. somewhere in an industrial factory) possible.

The block diagram (Fig.9) gives an example of how to use the FEEPROM with an 80C51 family microcontroller for remote downloading of firmware and parameter sets via a telephone line. The system consists of an 80C51/87C51 microcontroller, a PCF29F64 8 k x 8 FEEPROM, an RS232 driver, a MODEM and some glue logic.

The 80C51/87C51 contains firmware that has the following main tasks:

- MODEM control and handshaking (e.g. RTS/CTS or XON/XOFF)
- Protocol handling of downloaded file
- Programming control of FEEPROM

The addresses of the FEEPROM are mapped in such a way, that they are greater than the highest memory address of the microcontroller. For an 80C51/87C51 this will be 4 K. To achieve this an external address decoder is used. The erase mode of the FEEPROM is controlled by the level on the MODE pin. This pin is connected to an address decoder output in such a way, that for erasing a shadow 8 K memory area exists. Erasing can be performed by a correct write action to this memory area.

The $\overline{CE}$ signal for the FEEPROM is gated with the RESET of the microcontroller. The reason for this is to prevent unwanted write actions to the FEEPROM during power-up. This may occur when the power is already within the specified values, but the oscillator of the microcontroller has not yet started up. In this time frame the status of the microcontroller port pins is undefined.

By combining the microcontroller $\overline{RD}$ and $\overline{PSEN}$ signals, the PCF29F64 is accesible as both program memory and external data memory.

After power-on the program will start from the internal microcontroller program. This program will carry out some modem initialization and then jump to the user program in the PCF29F64. The interrupt vector addresses in the microcontroller must be remapped to the PCF29F64, so that execution of the user interrupt service routine is possible.
When data is about to be received (via the RS232 $\overline{DCD}$ line or is received (UART interrupt), the download program in the microcontroller is started. The received data file should be an absolute output file such as e.g. an INTEL Intellec-8 HEX file. During the download/programming time, interrupts that are mapped to the PCF29F64 address space, should be disabled to prevent unintentional jumps to the FEEPROM. When the communication is finished and all data programmed in the FEEPROM, the firmware in the microcontroller may jump again to the user program in the PFC29F64.

As previously mentioned, the PCF29F64 may be used as user program and external data memory. However, when the user program wants to program or erase FEEPROM location(s) in the same PCF29F64 device, program execution from this device is inhibited. A solution may be that the FEEPROM programming routines for the user program reside in the microcontroller program memory. Program execution should stay there in a loop, until programming or erasing of the PCF29F64 is finished. Remapped interrupts to a PCF29f64 device that will be programmed, should be disabled to prevent unintentional jumps to this device.
When program execution is carried out from the internal microcontroller memory, the AD0 to AD7 pins will float. To assure defined levels on the I/O0 to I/O7 pins of the FEEPROM, pull-up resistors are applied.

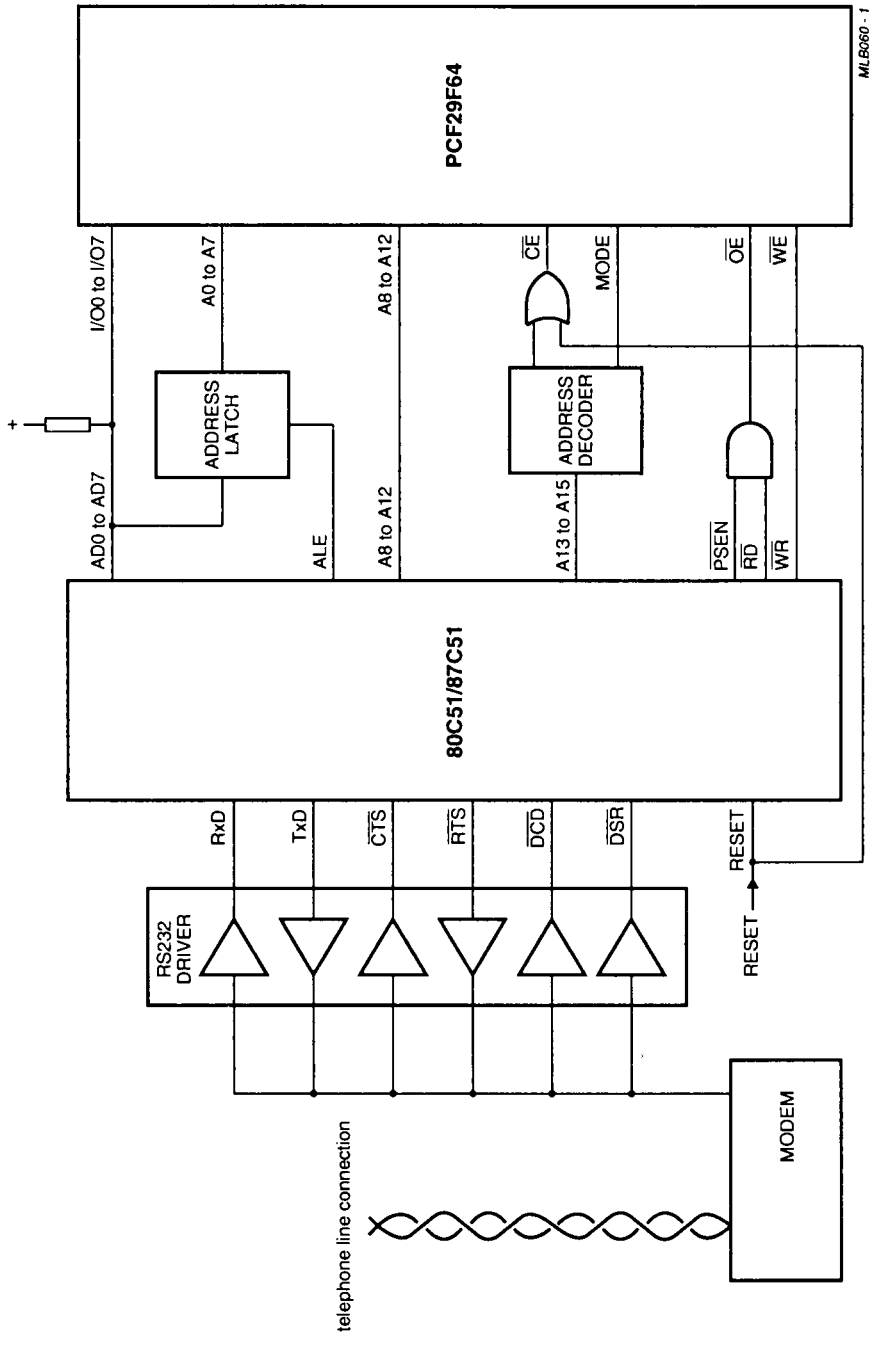
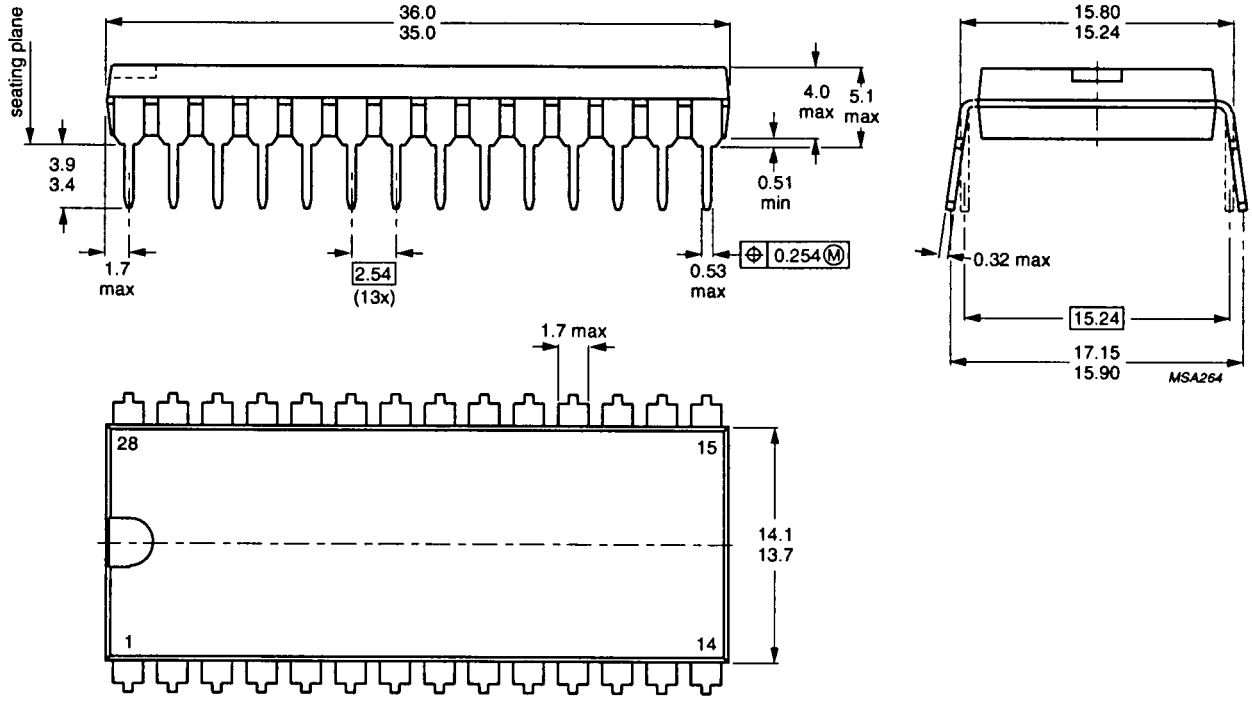


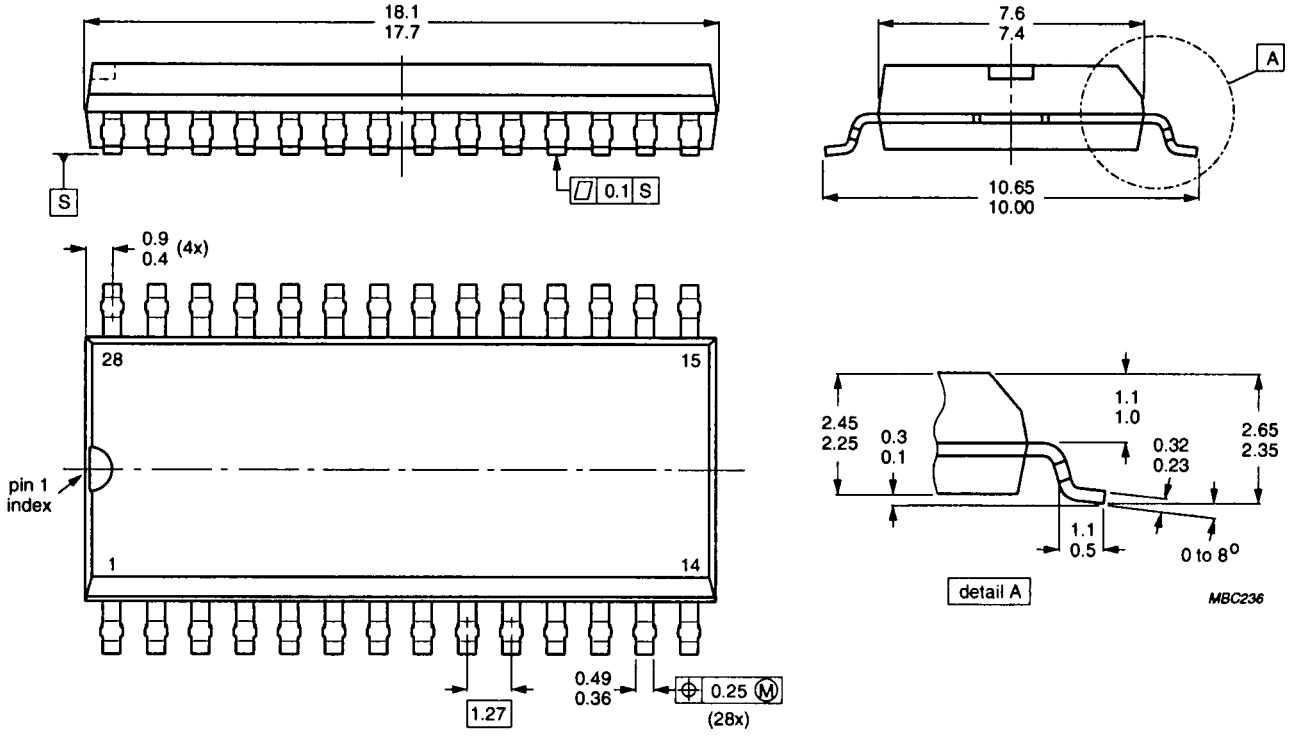
Fig.9 Application diagram.

PACKAGE OUTLINES



Dimensions in mm

Fig.10 28-lead dual in-line; plastic (SOT117).



Dimensions in mm

Fig.11 28-lead mini-pack; plastic (SO28; SOT136).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The devic may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

SOLDERING

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After cutting the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Philips Semiconductors – a worldwide company

Argentina IEROD, Juramento 1.991 - 14'B, 1428 Buenos Aires, Tel. (541)786-76-35, Fax. (541)786-93-67

Australia 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. (02)805 4455, Fax. (02)805 4466

Austria Triester Str. 64, 1101 WIEN, Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02)525 6111, Fax. (02)525 7246

Brazil Rua do Rocia 220, SAO PAULO-SP, CEP 04552, P.O. Box 7383-CEP 01051, Tel. (011)829-1166, Fax. (011)829-1849

Canada INTEGRATED CIRCUITS: Tel. (800)234-7381, Fax. (708)296-8556 DISCRETE SEMICONDUCTORS: 601 Milner Ave, SCARBOROUGH, ONTARIO, M1B 1M8, Tel. (416)292 5161 ext. 2336, Fax. (416)292 4477

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Colombia Carrera 21 No. 56-17, BOGOTA, D.E., P.O. Box 77621, Tel. (01)249 7624, Fax. (01)217 4549

Denmark Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. (32)88 2636, Fax. (31)57 1949

Finland Sinikalliontie 3, SF-02630 ESPOO, Tel. (0)50261, Fax. (0)520971

France 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01)4093 8000, Fax. (01)4093 8127

Germany Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040)3296-0, Fax. (040)3296 213

Greece No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01)4894 339/4894 911, Fax. (01)4814 240

Hong Kong 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)4245 121, Fax. (0)4806 960

India PEICO ELECTRONICS & ELECTRICALS LTD., Components Dept., Shivsagar Estate, Block 'A', Dr. Annie Besant Rd., Worli, BOMBAY-400 018, Tel. (022)4938 541, Fax. (022)4941 595

Indonesia Philips House, Jalan H.R. Rasuna Said Kav. 3-4, P.O. Box 4252, JAKARTA 12950, Tel. (021)5201 122, Fax. (021)5205 189

Ireland Newstead, Clonskeagh, DUBLIN 14, Tel. (01)640 000, Fax. (01)640 200

Italy V. Le F. Testi, 327, 20162-MILANO, Tel. (02)6752 2642, Fax. (02)6752 2648

Japan Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKIO 108, Tel. (03)3740 5101, Fax. (03)37400 570

Korea (Republic of) Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02)794-5011, Fax. (02)798-8022

Malaysia No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. (03)7755 1088, Fax. (03)757 4880

Mexico Philips Components, 6D Founder Blvd., EL PASO, TX 79906, Tel. (708)296-5462, Fax. (708)296-8556

Netherlands Postbus 90050, 5600 PB EINDHOVEN, Tel. (040)78 37 49, Fax. (040)78 83 99

New Zealand 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. (09)849-4160, Fax. (09)849-7811

Norway Box 1, Manglerud 0612, OSLO, Tel. (02)74 8000, Fax. (02)74 8341

Pakistan Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021)577 039, Fax. (021)569 1832

Peru Carretera Central 6.500, LIMA 3, Apartado 5612, Tel. (014)350 059, Fax. (014)468 999/468 949

Philippines PHILIPS SEMICONDUCTORS PHILIPPINES Inc, 106 Valero St. Salcedo Village, P.O. Box 911, MAKATI, Metro MANILA, Tel. (02)810 0161, Fax. (02)817 3474

Portugal Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (01)683 121, Fax. (01)658 013

Singapore Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. (65)350 2000, Fax. (65)251 6500

South Africa 195-215 Main Road, JOHANNESBURG 2000, P.O. Box 7430, Tel. (011)8893 911, Fax. (011)8893 191

Spain Balmes 22, 08007 BARCELONA, Tel. (03)301 6312, Fax. (03)301 4243

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