Blue Bird FPGA Development Kit

User Manual

Chapter 1

Chapter 2

Chapter 3

Chapter 1

1.1 Package content

Figure 1.1 shows a picture of the BlueBird FPGA kit (revision B)

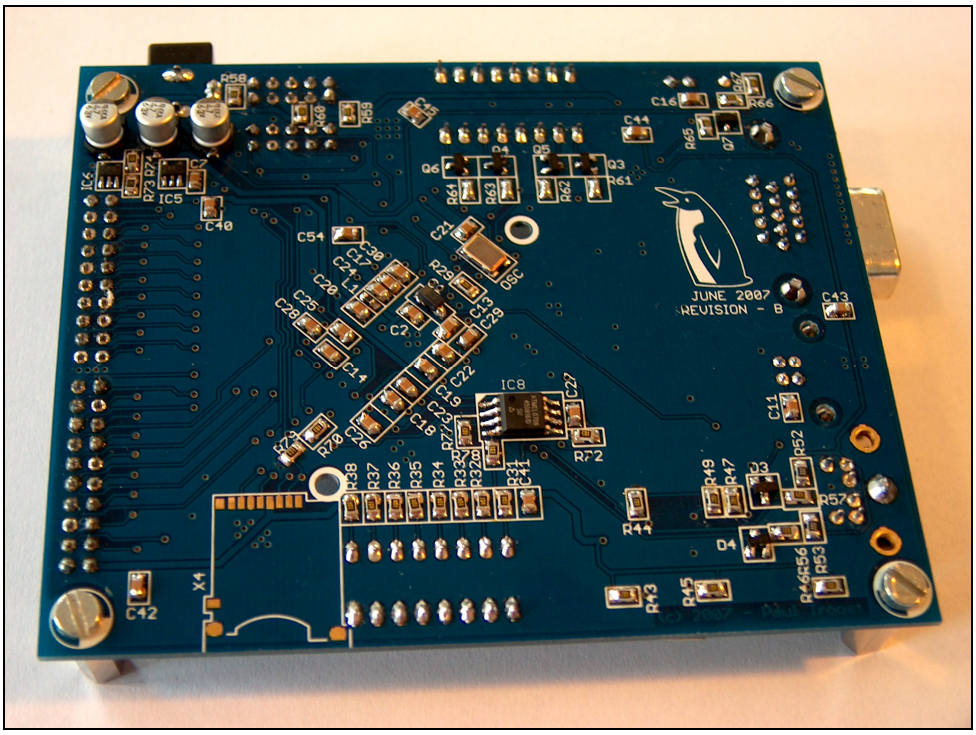

Figure 1.1 – The BlueBird FPGA kit package content.

The BlueBird FPGA kit includes:

- Revision 2 PCB
- Xxx
- Xxx
- Xxx
- Xxx
- Xxx
- Xxx
- Xxx
- Xxx

1.2 The BlueBird FPGA Kit Assembly

Please revere to the BlueBird FPGA Kit Assembly manual for assembly instructions.

1.3 Getting Help

The BlueBird project as a non/low-profit project intended for hobbyists with (some) experience in the field of embedded systems electronics . Due to the very limited profit, support is not guaranteed and may be limited.

If you do need help you may try the following addresses

Paul Troost
Hardware designer. Only for bugs or hardware related problems with the BlueBird.
Email: paul.troost@gmail.com

Samenkopen.net
Dutch site with shop and user based forum. Only intended for sales questions.
Address:
http://samenkopen.net/action/178562

CircuitsOnline.net
Dutch BBS (Bulletin Board System) which may give support on other (non-BlueBird) hardware and software problems.
Address: http://www.circuitsonline.net

Chapter 2

2.1 Layout and Components

A pothograph of a fully assembled BlueBird FPGA kit is shown in Figure 2.1. It depicts all the layout of the board and indicates connectors and key components.

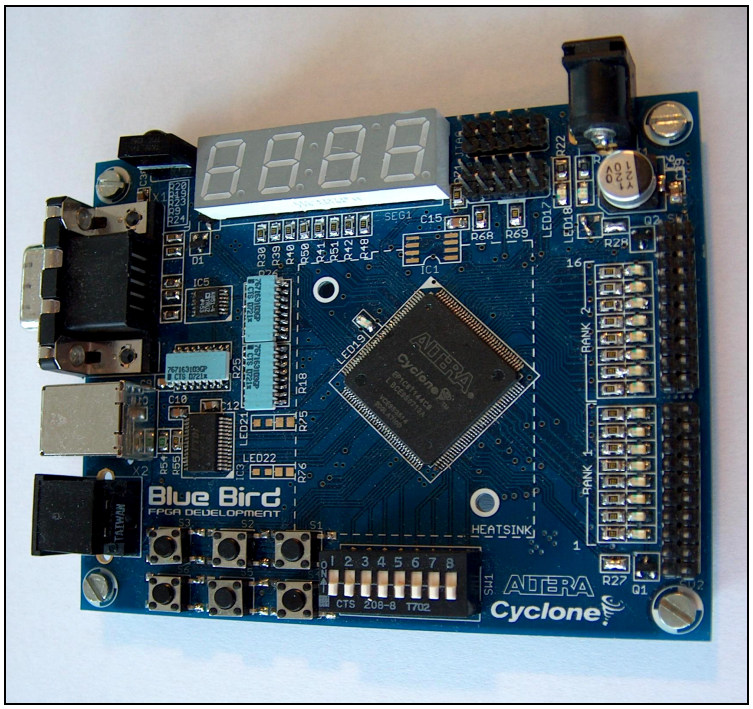

Figure 2.1 – Fully assembled BlueBird FPGA Kit (Revision B).

The BlueBird FPGA Kit has many features that allow the user to implement a wide range of designs. Ranging from simple circuits to complex multimedia projects.

The following hardware is provided on the BlueBird board:

- Altera Cyclone I 1C6 FPGA device
- Altera Serial Configuration device – EPCS4
- 16 Mbit of dataflash
- microSD card socket
- 6 pushbutton switches
- 8 toggle switches
- 16 red user LEDs
- 4 red 7 segment displays
- 50MHz oscillator
- R2R 6-bits VGA DAC with VGA-out connector
- USB to UART controller with USB B female connector
- PS/2 mouse/keyboard connector

- IrDA receiver (36kHz)
- Two 20 pins expansion headers
- JTAG and AS connector

In order to use the BlueBird FPGA board the user needs to be familiar with the Quartus II software. Tutorials for the Quartus II software may be found at:

- ftp://ftp.altera.com/up/pub/Tutorials/DE2/Digital_Logic/tut_quartus_intro_verilog.pdf
- ftp://ftp.altera.com/up/pub/Tutorials/DE2/Digital_Logic/tut_quartus_intro_vhdl.pdf
- ftp://ftp.altera.com/up/pub/Tutorials/DE2/Digital_Logic/tut_quartus_intro_schem.pdf

Tutorials are respectively for verilog design, vhdl design and schematic entry. Alternatively, a set of video tutorials is available to explain some features of the Quartus II software.

- http://www.altera.com/education/demonstrations/online/design-software/onl-design-software-demos.html

Also, a number of software examples is provided to show the basic and advanced capabilities of the BlueBird FPGA board.

2.2 Block Diagram of the BlueBird FPGA Board

Figure 2.2 gives the block diagram of the BlueBird FPGA board.

Figure 2.2 – Block diagram of the BlueBird FPGA board.

Following is more detailed information about the blocks in Figure 2.2:

Cyclone I 1C6 FPGA
- 5,960 LE's.
- 20 RAM Blocks (4kBits + parity).
- 92,160 RAM Bits.
- 2 PLLs.
- 98 User IO pins.
- Thin Quad Flat Pack 144 pins package.

Serial Configuration
- Altera's EPCS4 Serial Configuration Device.
- 4Mbit memory size.
- JTAG and AS programming modes are supported.

Flash Data memory

- 16 Mbit Flash memory.
- SPI protocol.

microSD Card Socket

- Provides SPI access to microSD cards.

Pushbutton switches

- 6 Pushbuttons.
- Normally high, low when pressed.
- **Not** denounced.

Toggle Switches

- 8 Toggle switches.
- A switch causes a logic 0 when in the UP position (indicated by ON arrow) and a logic 1 in the DOWN position).

Clock Input

- 50 MHz oscillator.
- 48 MHz oscillator.

VGA Output

- Uses 6-bit R2R DAC for 64 colours.
- Max resolution of 800x600 @ 85Hz or 1024x768 @ 60Hz.

USB Device

- Complies fully with USB Specifications rev 2.0.
- Supports transfer rates from 300 baud to 1 Megabaud.
- FTDIChip-ID™ Security Dongle.
- Support bit banging.

IrDA Receiver

- Contains an 36kHz IR receiver.

Two 20 Pins Expansion Headers

- 36 Cyclone I I/O pins and 4 power (3V3) and ground pins.
- 40 pins header accepts 0.1” pitched connectors
- **No** protection!

2.3 Power-up The BlueBird FPGA board

The BlueBird FPGA Board comes with an preloaded bit stream to demonstrate some of the features of the board. This bit stream allows user to see quickly if the board is functioning correctly. To power-up the board, perform the following steps:

1. Connect and 5V adapter with an 2.1mm jack to the board (do not plug into wall socket). The adapter should be able to deliver at least 500mA and output voltage should be with ±2% (4.9V to 5.1V).
2. Connect a VGA monitor to the VGA port on the BlueBird board
3. Connect a PS/2 keyboard to the PS/2 port on the BlueBird board
4. Connect the BlueBird board with an USB A male - B male cable to an PC
5. Optionally, connect an programmer to the JTAG port. For communication between the BlueBird board and the host PC you need to have installed the altera driver software for ByteBlaster or USBBlaster.
6. Plug in adapter to power on the BlueBird FPGA board.

At this point you should observe the following

- All user LEDs are flashing.
- All 7 segments are cycling through 0 to F.
- The VGA monitor display's a welcome screen.
- Toggle switch SW1 to invert LED bank 2.
- Host PC should find a new USB device named 'BlueBird FPGA Board'

Figure 2.3 – Default VGA output pattern

Chapter 3

3.1 Configuring the Cyclone I FPGA

The procedure for downloading the design from a host computer to the BlueBird FPGA board is descripted in the tutorial *Quartus II introduction*. See section 2.2 for the location of this tutorial. The user is encouraged to read the tutorial first, and to treat the information below as a short reference.

The BlueBird FPGA Board contains a serial EEPROM chip that stores the configuration data for the Cyclone I FPGA. This configuration is automatically loaded from the EEPROM chip into the Cyclone I FPGA when power is applied to the board. Using the Quartus II software, it is possible to reprogram the FPGA at any time. And it is also possible to change to non-volatile data that is stored in the serial EEPROM chip. Both types of programming methods are described below:

1. JTAG programming. In this method of programming the configuration bit stream is loaded directly into the Cyclone I FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration is lost when the power is turned off.
2. AS programming. In this method of programming the configuration bit stream is loaded in the EPCS4 serial EEPROM chip. It provides non-volatile storage for the bit stream so that the information is retained, even when the power is turned off. When the power is turned on, the configuration data in the EPCS4 is automatically loaded into the Cyclone I FPGA.

The sections below describe the steps used to perform both JTAG and AS programming. For both methods you need to have access to an ByteBlaster (MV/II) or USBBlaster and have the proper drivers installed. Tutorials on installing an ByteBlaster or USBBlaster may be found on altera's website.

- http://www.altera.com/literature/ug/ug_bbii.pdf (ByteBlaster II)
- http://www.altera.com/literature/ug/ug_bbmv.pdf (ByteBlaster MV)
- http://www.altera.com/literature/ug/ug_usb_blstr.pdf (USBBlaster)

Configuring the FPGA in JTAG mode

To download a configuration bit stream into the Cyclone I FPGA, perform the following steps.

1. Ensure that power is supplied to the BlueBird FPGA Board
2. Connect the ByteBlaster or USB Blaster to the JTAG header (see Figure 2.1)

3. The FPGA can now be programmed by using the Quartus II Programmer module (*Tools -> Programmer*). Select an configuration bit file with the **.sof* extension and select your hardware. Press 'Start Programming' to start programming the FPGA.

Configuring the EPCS4 in AS mode

To download a configuration bit stream into the EPCS4 serial EEPROM chip, perform the following steps:

1. Ensure power is supplied to the BlueBird FPGA Board
2. Connect the ByteBlaster or USB Blaster to the AS header (see Figure 2.1)
3. The FPGA can now be programmed by using the Quartus II Programmer module (*Tools -> Programmer*). Select an configuration bit file with the **.pof* extension and select your hardware. Press 'Start Programming' to start programming the FPGA
4. Now reset the board by turning of the power for ±15 seconds. When power is again applied to the board, the new configuration data will be loaded from the EPCS4 into the Cyclone I FPGA.

In addition to using the JTAG header for programming, the JTAG header can also be used for other functions like the Signal Tap® II function from Quartus II.

3.2 Using the LEDs and switches

The BlueBird FPGA board provides six pushbutton switches, AS indicated in Figure 3.1, non of these switches are debounced and thus should not be used as clock or reset inputs.
Each switch provides a high logic level (3.3 volt) when it is not pressed and a low logic level (0 volts) when pressed.

Figure 3.1 – No debouncing

There are also 8 toggle switches on the BlueBird FPGA Board. These switches are also not debounced and are intended for use as level-sensitive data inputs to a circuit. When a switch is in the DOWN position it provides a high logic level (3.3 volts) to the FPGA, and when the switch is in the UP position (indicated by the ON arrow) it provides a low logic level (0 volts) to the FPGA.

There are 16 user-controllable LEDs on the BlueBird FPGA board. All 16 LEDs are found on the right side of the board, next to the expansion headers. The LEDs are arranged in 2 banks of 8 LEDs that can be individually enabled. Each LED is driven directly by a pin on the Cyclone I FPGA; driving its associated pin to high logic turns the LED on, and driving it to logic low turns it off.
A schematic diagram that show the pushbutton and toggle switches is given in Figure 3.2. A schematic diagram that shows the LED circuitry appears in Figure 3.3

A list of the pin names on the Cyclone I FPGA that are connected to the toggle switches is given in Table 3.1. Similarly, the pins used to connect the pushbutton switches and LEDs are displayed in Tables 3.2 and 3.3, respectively.

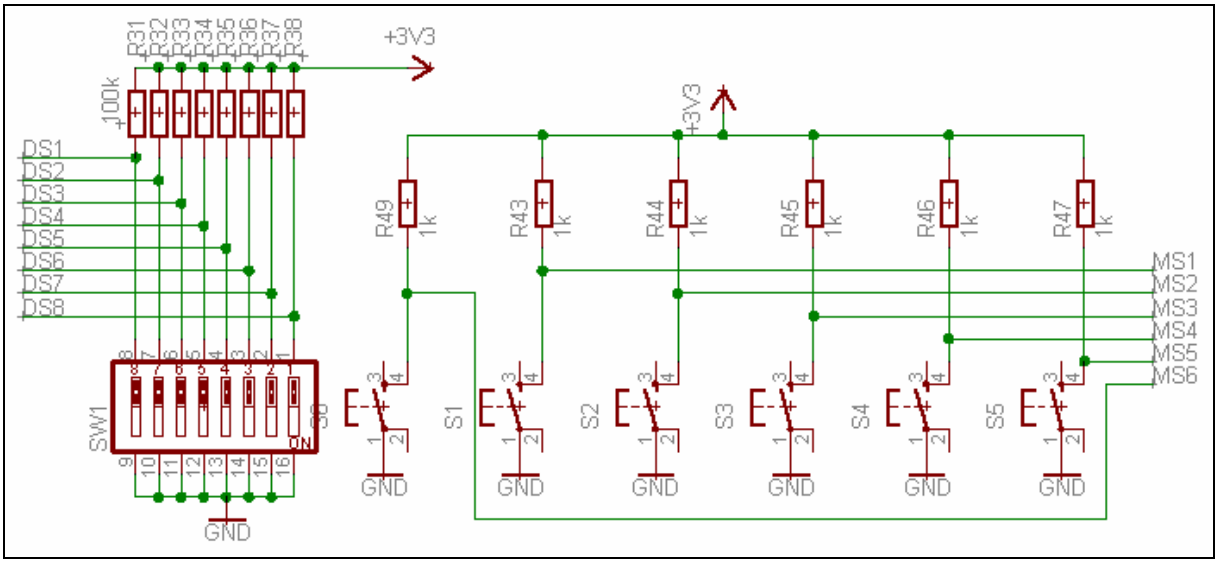

Figure 3.2 – Schematic diagram of the pushbutton and toggle switches.

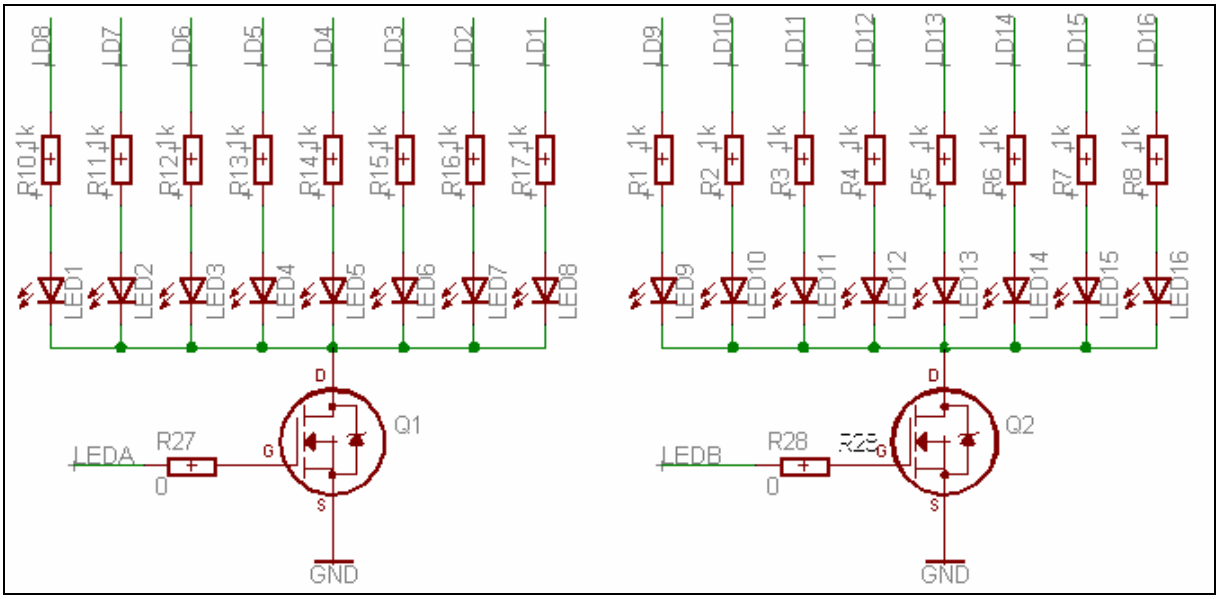

Figure 3.3 – Schematic diagram of the LEDs.

Signal Name	FPGA Pin No.	Description
DS1	PIN_69	Toggle Switch 1
DS2	PIN_70	Toggle Switch 2
DS3	PIN_71	Toggle Switch 3
DS4	PIN_72	Toggle Switch 4
DS5	PIN_73	Toggle Switch 5
DS6	PIN_74	Toggle Switch 6
DS7	PIN_75	Toggle Switch 7
DS8	PIN_76	Toggle Switch 8

Table 3.1 – Pin assignments for the toggle switches.

Signal Name	FPGA Pin No.	Description
MS1	PIN_68	Push Button 1
MS2	PIN_61	Push Button 2
MS3	PIN_67	Push Button 3
MS4	PIN_62	Push Button 4
MS5	PIN_59	Push Button 5
MS6	PIN_60	Push Button 6

Table 3.2 – Pin assignments for the pushbutton switches.

Signal Name	FPGA Pin No.	Description
LD1	PIN_98	Led 1
LD2	PIN_100	Led 2
LD3	PIN_104	Led 3
LD4	PIN_106	Led 4
LD5	PIN_108	Led 5
LD6	PIN_110	Led 6
LD7	PIN_112	Led 7
LD8	PIN_114	Led 8
LD9	PIN_120	Led 9
LD10	PIN_122	Led 10
LD11	PIN_124	Led 11
LD12	PIN_128	Led 12
LD13	PIN_130	Led 13
LD14	PIN_132	Led 14
LD15	PIN_134	Led 15
LD16	PIN_140	Led 16
LEDA	PIN_83	Enable bank 1
LEDB	PIN_144	Enable bank 2

Table 3.3 – Pin assignments for the LEDs

3.3 Using the 7-segment displays

The BlueBird FPGA Board has four 4-segment displays. These displays are multiplexed, with the intent of displaying numbers of various sizes. AS indicated in the schematic of Figure 3.4, the seven segments are connected to pins on the Cyclone I FPGA. Applying a high logic level causes it to light up, and applying a low logic level turns it off.

Each segment in a display is identified by an index from A to 7, with its position given in figure 3.5. Note that the dot in each display is identified by index DP. Note that the middle two dots in the display are unconnected and cannot be used. Table 3.4 shows the assignments of FPGA pins to the 7-segment displays.

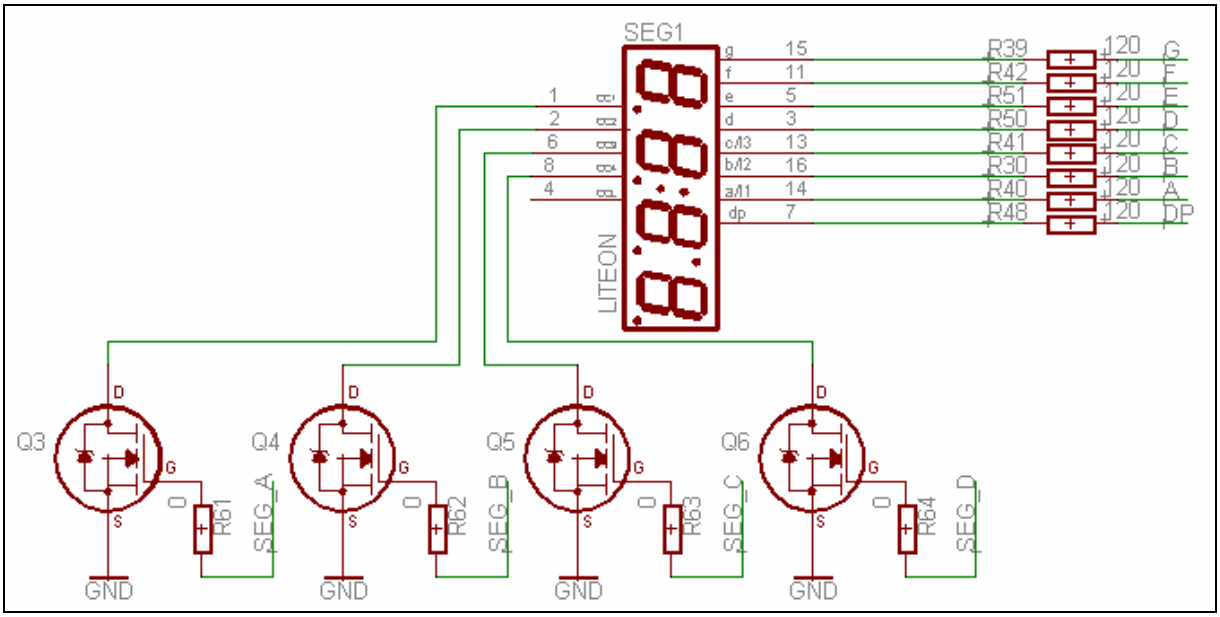

Figure 3.4 – Schematic diagram for 7-segment displays.

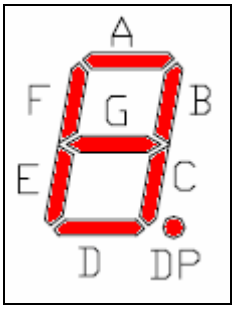

Figure 3.5 – Position and index of each segment in a 7-segment display

Signal Name	FPGA Pin No.	Description
A	PIN_10	Segment A
B	PIN_52	Segment B
C	PIN_5	Segment C
D	PIN_7	Segment D
E	Pin_4	Segment E

F	PIN_2	Segment F
G	PIN_51	Segment G
DP	PIN_1	Segment DP
SEG_A	PIN_26	Digit 1
SEG_B	PIN_11	Digit 2
SEG_C	PIN_6	Digit 3
SEG_D	PIN_3	Digit 4

Table 3.4 – Pin assignments for the 7-segment displays.

3.4 Clock Inputs

The BlueBird FPGA Board includes two oscillators. One that produces an 50 MHz clock signal. Another 48 MHz oscillator is active when an USB connection is available. The schematic for the clock circuitry is shown in Figure 3.6, and the associated pin assignments appears in Table 3.5.

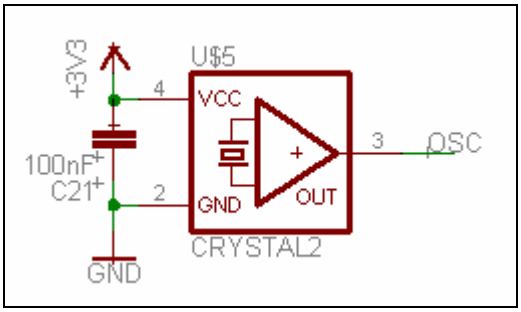

Figure 3.6 – Schematic diagram for the clock circuitry.

Signal Name	FPGA Pin No.	Description
OSC	PIN_16	50 MHz clock input
OSCO	PIN_17	48 MHz clock input

Table 3.5 – Pin assignments for the clock circuitry.

3.5 Using the Expansion Header

The BlueBird FPGA Board provides two 20-pins expansion headers. Each header connects directly to 18 pins on the Cyclone I FPGA, and also provides DC +3.3V and GND pins. Figure 3.7 shows the related schematics. 8 expansion pins per header from the FPGA are shared between user LEDs and the expansion header. When the user LEDs are enabled, a LED with an 1kΩ resistor is placed parallel to each of the 8 expansion pins. Table 3.6 shows pin assignments for the expansion headers.

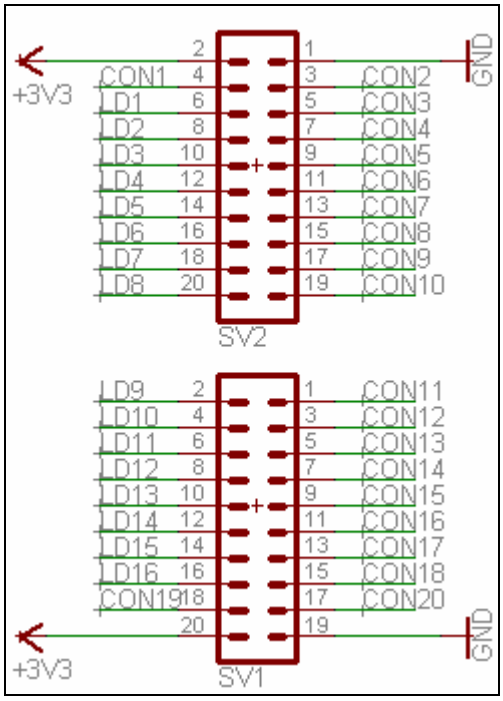

Figure 3.7 – Schematic diagram for the expansion headers

Signal Name	FPGA Pin No.	Description
CON1	PIN_84	GPIO Bank1
CON2	PIN_85	GPIO Bank1
LD1	PIN_98	GPIO Bank1
CON3	PIN_96	GPIO Bank1
LD2	PIN_100	GPIO Bank1
CON4	PIN_103	GPIO Bank1
LD3	PIN_104	GPIO Bank1
CON5	PIN_105	GPIO Bank1
LD4	PIN_106	GPIO Bank1
CON6	PIN_107	GPIO Bank1
LD5	PIN_108	GPIO Bank1
CON7	PIN_109	GPIO Bank1
LD6	PIN_110	GPIO Bank1
CON8	PIN_111	GPIO Bank1
LD7	PIN_112	GPIO Bank1
CON9	PIN_113	GPIO Bank1
LD8	PIN_114	GPIO Bank1
CON10	PIN_119	GPIO Bank1
LD9	PIN_120	GPIO Bank2
CON11	PIN_121	GPIO Bank2
LD10	PIN_122	GPIO Bank2
CON12	PIN_123	GPIO Bank2
LD11	PIN_124	GPIO Bank2
CON13	PIN_125	GPIO Bank2
LD12	PIN_128	GPIO Bank2

CON14	PIN_129	GPIO Bank2
LD13	PIN_130	GPIO Bank2
CON15	PIN_131	GPIO Bank2
LD14	PIN_132	GPIO Bank2
CON16	PIN_133	GPIO Bank2
LD15	PIN_134	GPIO Bank2
CON17	PIN_139	GPIO Bank2
LD16	PIN_140	GPIO Bank2
CON18	PIN_141	GPIO Bank2
CON19	PIN_142	GPIO Bank2
CON20	PIN_143	GPIO Bank2

Table 3.6 – Pin assignments for expansion headers.

3.6 Using VGA

The BlueBird FPGA Board includes a 16-pins HD D-SUB connector for VGA output. The VGA synchronization signals are provided directly from the Cyclone I FPGA. An R2R DAC with Analog Devices ADA4851 high speed video buffers are used to produce the analog data signals (red, green and blue). The associated schematic is given in Figure 3.8 and can support resolutions of up to 1024 x 768 pixels at 60Hz refresh rate.

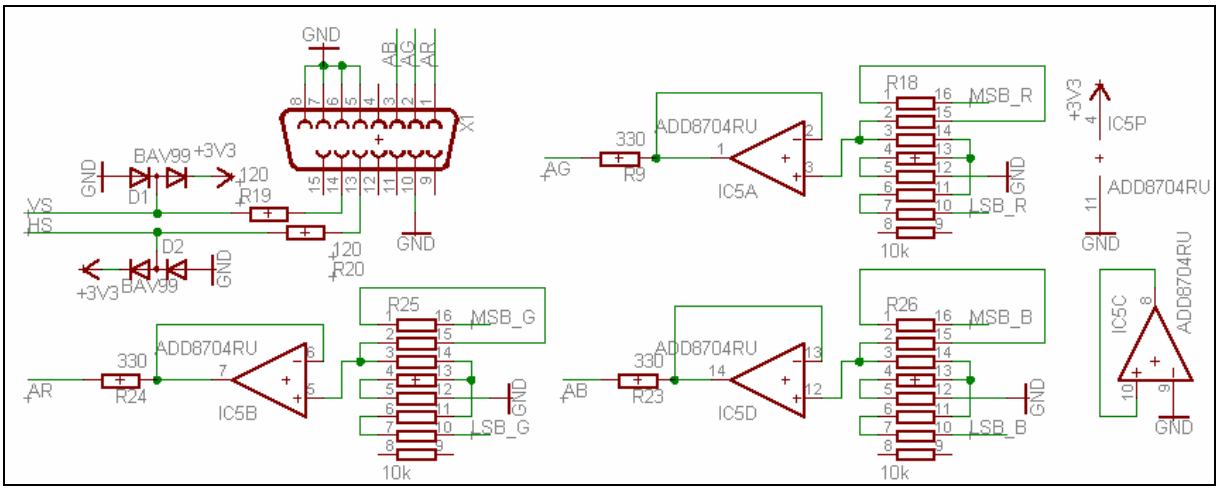

Figure 3.8 – Schematic diagram for the VGA circuit.

The timing specification for VGA synchronization and RGB data can be found on various educational web sites. Figure 3.9 illustrates the basic timing requirements for each row (horizontal) that is displayed on a VGA monitor. An active-low pulse of specific duration (time *a* in the figure) is applied to the horizontal synchronization (*hsync*) input of the monitor, which signifies the end of one row of data and the start of the next. The data (RGB) input on the monitor must be driven low for a time period called the **back porch** (*b*) after the *hsync* pulse occurs, which is followed by the display interval (*c*). During the data display interval the RGB data drives each pixel in turn across the row being displayed. Finally, there is a

time period called the **front porch** (*d*) where the data (RGB) inputs must again be off before the next *hsync* pulse can occur. The timing of the vertical synchronization (*vsync*) is the same as shown in Figure 3.9, except that a *vsync* pulse signifies the end of one frame and the start of the next, and the refers to the set of rows in the frame. Tables 3.7 and 3.8 show, for different resolutions, the durations of time periods *a*, *b*, *c* and *d* for both horizontal and vertical timing.

The pin assignments between the Cyclone I FPGA and the R2R DAC and ADA4581 are listed in Table 3.9.

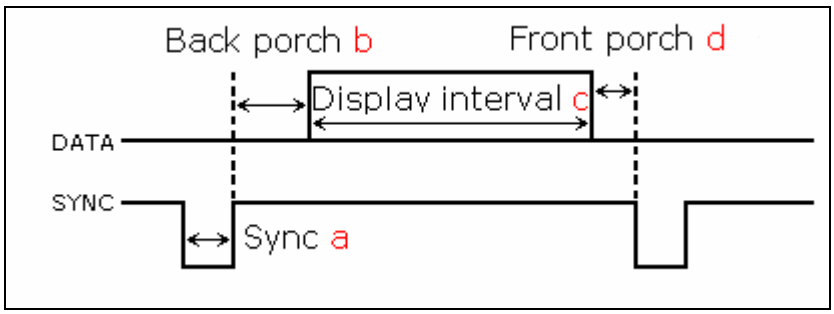

Figure 3.9 – VGA timing specification

VGA Mode		Horizontal Timing Spec.				
Configuration	Resolution	a (pixels)	b (pixels)	C (pixels)	D (pixels)	Pixel clock
VGA (60Hz)	640x480	96	48	640	15	25 MHz
VGA (85Hz)	640x480	58	79	640	58	36 MHz
SVGA (60Hz)	800x600	128	88	800	40	40 MHz
SVGA (75Hz)	800x600	79	158	800	15	49 MHz
SVGA (85Hz)	800x600	62	152	800	34	56 MHz
XGA (60Hz)	1024x768	136	162	1024	26	65 MHz
XGA (70Hz)	1024x768	135	142	1024	23	75 MHz
XGA (85Hz)	1024x768	95	209	1024	47	95 MHz

Table 3.7 – VGA horizontal timing specification

VGA Mode		Vertical Timing Spec.			
Configuration	Resolution	a (lines)	b (lines)	c (lines)	d (lines)
VGA (60Hz)	640x480	2	33	480	10
VGA (85Hz)	640x480	3	25	480	1
SVGA (60Hz)	800x600	4	23	600	1
SVGA (75Hz)	800x600	3	21	600	1
SVGA (85Hz)	800x600	3	27	600	1
XGA (60Hz)	1024x768	6	29	768	3
XGA (70Hz)	1024x768	6	29	768	3
XGA (85Hz)	1024x768	3	36	768	1

Table 3.8 – VGA vertical timing specification

Signal Name	FPGA Pin No.	Description

HS	PIN_28	Horizontal sync
VS	PIN_31	Vertical sync
MSB_R	PIN_34	**M**ost **S**ignificant **B**it Red
LSB_R	PIN_35	**L**east **S**ignificant **B**it Red
MSB_G	PIN_36	MSB Green
LSB_G	PIN_37	LSB Green
MSB_B	PIN_32	MSB Blue
LSB_B	PIN_33	LSB Blue

Table 3.9 – VGA pin assignments.

3.7 USB Port

The BlueBird FPGA Board provides USB device interface using the FT232RL single-chip USB controller. The device controller is compliant with the Universal Serial Bus Specification Rev 2.0, supporting data transfer at 1 MegaBaud. Figure 3.10 shows the schematic diagram of the USB circuitry; the pin assignments for the associated interface are listed in Table 3.10.

Detailed information using the FT232RL device is available in its datasheet and programming guide; both can be found on the manufacturer's website:

- http://www.ftdichip.com/Documents/AppNotes.htm
- http://www.ftdichip.com/Documents/Articles.htm
- http://www.ftdichip.com/Documents/ProgramGuides.htm

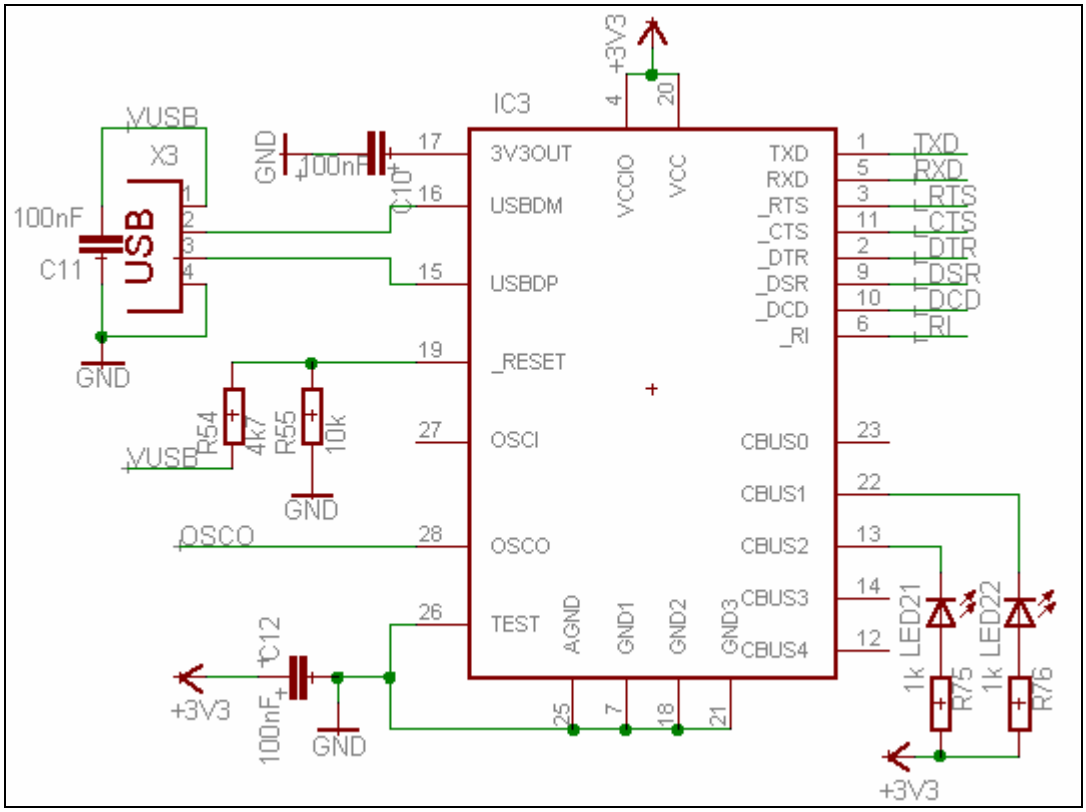

Figure 3.10 – Schematic diagram for USB circuitry.

Signal Name	FPGA Pin No.	Description
TXD	PIN_49	Transmit data output
RXD	PIN_42	Receive data input
_RTS	PIN_47	Request to send
_CTS	PIN_38	Clear to send
_DTR	PIN_48	Data terminal ready
_DSR	PIN_40	Data set ready
_DCD	PIN_39	Data carrier detect
_RI	PIN_41	Ring indicator

Table 3.10 – Pin assignments for USB circuitry.

3.8 PS/2 Port

The Blue Bird FPGA Board includes a standard PS/2 interface and a connector for a PS/2 keyboard or mouse. Figure 3.11 shows the schematic of the PS/2 circuit. The pin assignments for the associated interface are shown in Table 3.10.

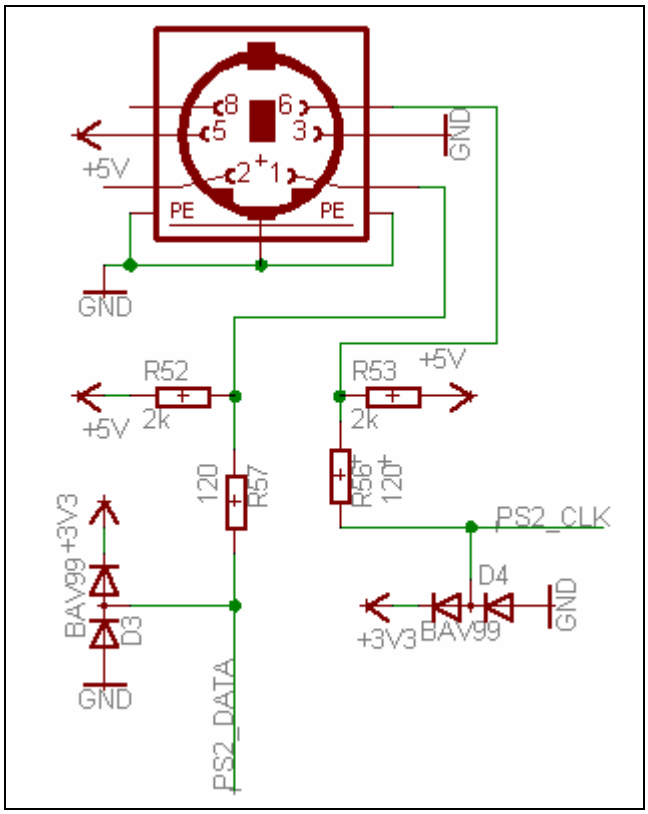

Figure 3.11 – Schematic diagram for PS/2 Port.

Signal Name	FPGA Pin No.	Description
PS2_DATA	PIN_57	PS/2 Data
PS2_CLK	PIN_58	PS/2 Clock

Table 3.11 – PS/2 Port pin assignments.

3.9 Using IrDA

The BlueBird FPGA Board provides a simple wireless communication media using an TSOP1736 infrared receiver. For more information, refer to the datasheet for this device. Figure 3.12 shows the schematic for the IrDA communication link. The pin assignment of the interface is listed in Table 3.12.

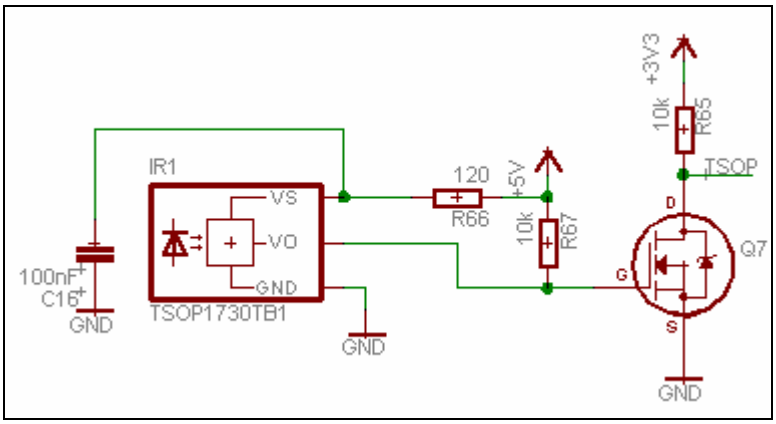

Figure 3.12 – Schematic diagram for IrDA circuit.

Signal Name	FPGA Pin No.	Description
TSOP	PIN_27	RX Data

Table 3.12 – Pin assignments for IrDA

3.10 Using Flash

De BlueBird FPGA Board provides 16Mbit data flash using the AT45DB161D. Figure 3.13 shows the schematic for the memory chip. Table 3.13 shows the pin assignments.

More information about using the AT45DB161D may be found in the datasheet:

- http://www.atmel.com/dyn/resources/prod_documents/doc3500.pdf

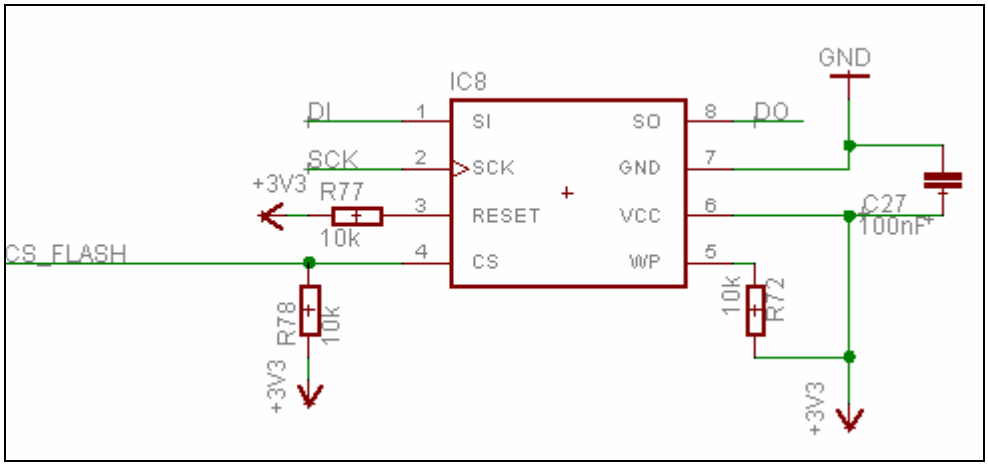

Figure 3.13 – Schematic diagram for data flash.

Signal Name	FPGA Pin No.	Description
CS_FLASH	PIN_77	Chip select
DI	PIN_78	Data input
DO	PIN_82	Data output
SCK	PIN_79	Serial clock

Table 3.13 – Pin assignments for data flash.