(12) **UK Patent Application** (19) **GB** (11) **2 219 900** (13)A

(43) Date of A publication 20.12.1989

(21) Application No 8814091.8

(22) Date of filing 14.06.1988

(71) Applicant
ABI Systems Limited

(Incorporated in the United Kingdom)

3 Quineys Road, Shottery, Stratford upon Avon, Warwickshire, CV37 9BW, United Kingdom

(72) Inventor
Bernard Bollons

(74) Agent and/or Address for Service
Anthony Cundy & Co
384 Station Road, Dorridge, Solihull, West Midlands, B93 8ES, United Kingdom

(51) INT CL⁴
H03F 1/08, H03B 5/24, H03F 3/45

(52) UK CL (Edition J)
**H3T** TKF TVP T1G3R T2T2Z T3N T3V T3X T6PX T6P2
U1S S1947

(56) Documents cited
GB 2069269 A   **GB 2038127 A**   **GB 1339933 A**
GB 1213110 A   **GB 1142894 A**   **GB 1020286 A**
"Electronics" October 28th 1968 page 90

(58) Field of search
UK CL (Edition J) H3T TUS TVP TVX
INT CL⁴ H03F

(54) **Zero input capacitance amplifier**

(57) An ampifier includes a first integrated circuit differential amplifier (IC2), the output of the first differential amplifier (IC2) being fed back to its inverting input, an input is applied to its non-inverting input and second and third differential amplifiers (IC1 and IC3) are provided in the positive (+VS) and negative (-VS) supply line by which the input signal to the first differential amplifier (IC2) may be imposed on the positive (+VS) and negative (-VS) supplies, so that the input capacitance of the first differential amplifier (IC2) is effectively zero.

FIG 1

GB 2 219 900 A

2219900

FIG 2

FIG 1
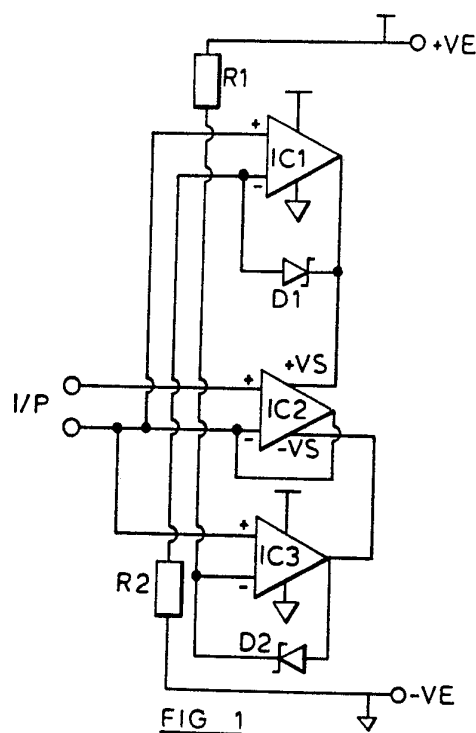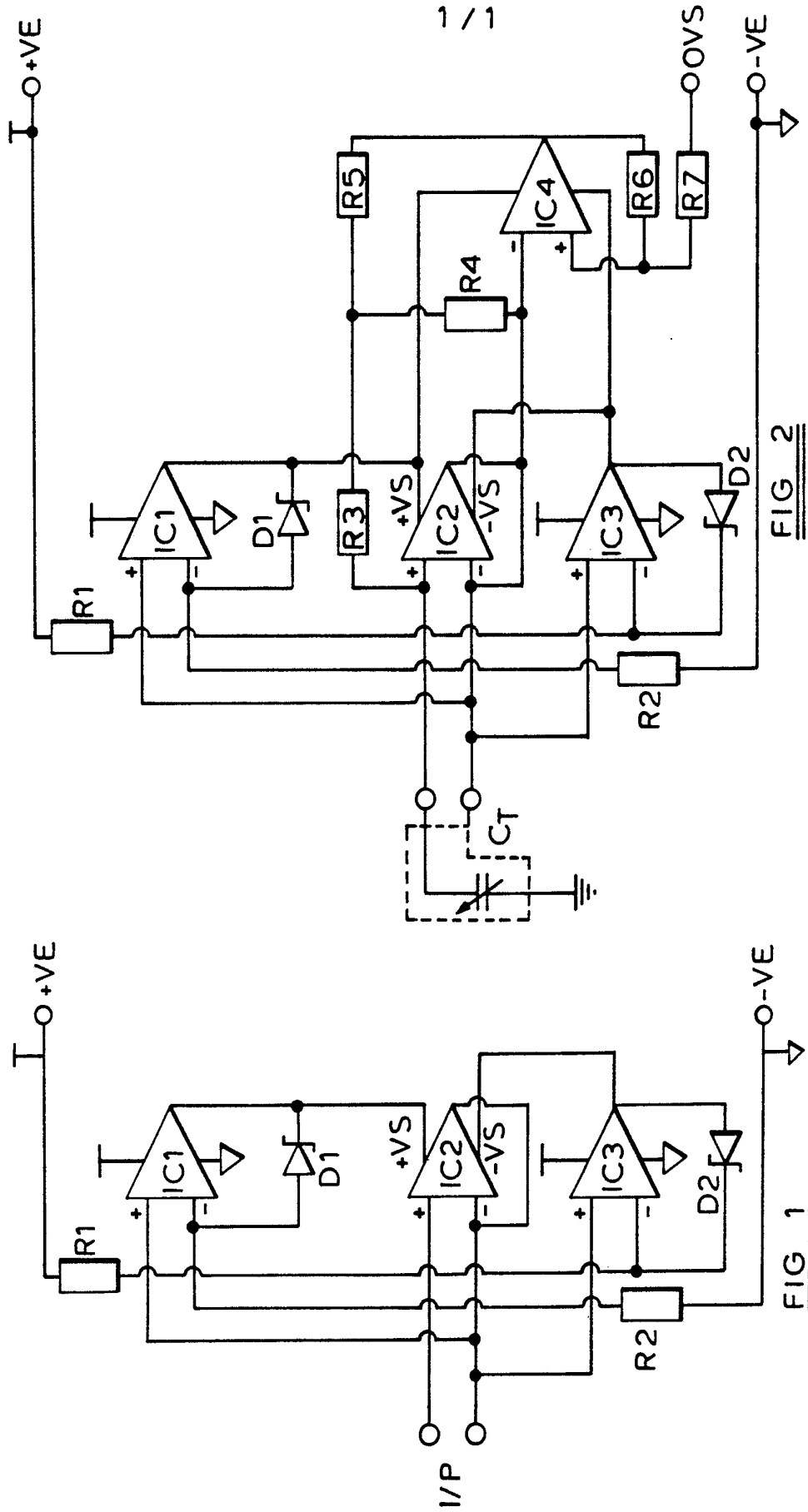
AMPLIFIERS

The present invention relates to amplifiers and to circuits including such amplifiers.

Modern integrated circuit differential amplifiers exhibit very high input impedence and very low drift with variation
05 in temperature. Buffer amplifiers are conventionally formed from a differential amplifier configured as a voltage follower in which the output of a differential amplifier is connected to the inverting input and an input signal is applied to the non-inverting input.

10 However, with integrated circuit differential amplifiers, because of inherent inter-track capacitance imposed by the physical makeup of the circuit, the differential amplifier will have an input capacitance, typically 1.5 pF. This input capacitance is due, in the main, to capacitive
15 coupling between the non-inverting input and the positive and negative supply lines.

This input capacitance does not normally present any problem when the amplifier is used in conventional applications. However for very specialised designs, eg.
20 precision capacitance measuring systems this small input capacitance will cause unacceptable non-linearities,

therefore an amplifier with zero input capacitance is desirable.

The present invention provides an amplifier with effectively zero input impedence.

05   According to one aspect of the present invention an amplifier comprises a first integrated circuit differential amplifier, the output of the differential amplifier being fed back to its inverting input, an input being applied to its non-inverting input and means being provided in the
10   positive and negative supply lines by which the input signal to the differential amplifier may be imposed on the positive and negative supplies.

By imposing the input signal on the positive and negative supplies in the manner described above, the positive and
15   negative supplies will rise and fall with the input and consequently there will be no current to charge the capacitive coupling therebetween and as a result the input capacitance of the amplifier will be effectively zero.

The amplifier described above is particularly suitable for
20   producing a capacitance to frequency converter.

According to one further aspect of the present invention a capacitance to frequency converter comprises an amplifier (as hereinbefore defined) the output of the first differential amplifier being connected to the inverting

05 input of a further integrated circuit differential amplifier, the further differential amplifier being configured as a Schmitt trigger, common positive and negative voltage supplies being applied across the first and further differential amplifiers.

10 Various embodiments of the invention are now described, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 shows a circuit diagram of a buffer amplifier formed in accordance with the present invention; and

15 Figure 2 shows a circuit diagram of a capacitance to frequency converter based on the buffer amplifier shown in figure 1.

As illustrated in Figure 1 a buffer amplifier comprises a differential amplifier IC2, the output of which is

20 connected to its inverting input. The output from the differential amplifier IC2 is also connected to the

non-inverting inputs of second and third differential amplifiers IC1 and IC3. The outputs of IC1 and IC3 are fed back to their inverting inputs via zener doides D1 and D2 respectively. The inverting input of amplifier IC1 is

05 connected to the negative voltage source (-VE) via resistance R2 and the inverting input amplifier IC3 is connected to the positive voltage source (+VE) via resistance R1. The positive voltage supply (+VS) to amplifier IC2 is taken from the output of amplifier IC1

10 while the negative voltage supply (-VS) is taken from the output of amplifier IC3. An input signal to the buffer amplifier is applied to the non-inverting input of amplifier IC2.

With this circuit, there is feedback action which causes

15 the inverting inputs of amplifiers IC1 and IC3 to track the output of amplifier IC2. The network R2,D1 ensures that the zener diode D1 is conducting at its reference voltage and therefore that the output of amplifier IC1 will be more positive than the output of amplifier IC2 by the reference

20 voltage of zener diode D1. Similarly, the output voltage of amplifier IC3 will be more negative than the output of amplifier IC2 by the reference voltage of zener diode D2.

Consequently a constant voltage supply equal to sum of the reference voltages of zener diodes D1 and D2 will be

applied across the amplifier IC2, but the positive and negative supplies (+VS) and (-VS) will go up and down with the input signal. As a result, there will be no variation of potential between the input signal of IC2 and its supply
05 connections, therefore there will be no signal current charging the input capacitance which exists between the input of the amplifier IC2 and its supply connections

The proposed circuit consequently avoids the input capacitance which is inevitable with conventional
10 integrated circuit differential amplifiers.

In the capacitance to frequency converter illustrated in Figure 2, the output from differential amplifier IC2 of the buffer amplifier illustrated in Figure 1, is connected to the inverting input of a further differential amplifier
15 IC4. The output from amplifier IC4 is connected to; the non-inverting input of amplifier IC4 via resistance R6, the non-inverting input for amplifier IC2 via resistances R3 and R5, the inverting input of amplifier IC4 via resistances R4 and R5 and to a zero voltage supply (0VS)
20 via resistances R6 and R7. The non-inverting input of amplifier IC4 is connected to the zero voltage supply (0VS) via resistance R7.

An output is taken from between the output of amplifier IC4

and the zero voltage supply (OVS) and an input, for example from a variable capacitive device Ct, is applied to the non-inverting input of IC2. The inverting input of IC2 may be connected to a screen of the input cable. The positive

05 and negative supplies to amplifier IC4 are taken from the outputs of amplifiers IC1 and IC3 respectively.

The amplifier IC4 is configured as a Schmitt Trigger. The output of IC4 will always be either hard positive (+VS) or hard negative (-VS). Consequently a fraction of either the

10 positive or negative supplies (+VS) or (-VS), will always appear across resistance R4. Since the output of amplifier IC2 will be at the same potential as the input, a constant voltage will be imposed on resistance R3 and therefore a constant current (I) will flow through resistance R3. This

15 constant current will charge capacitive device Ct and hence a voltage ramp will occur at the output of amplifier IC2. Amplifier IC4 will toggle from the positive supply voltage (+VS) to the negative supply voltage (-VS) as the ramp reaches the limit of the hysteresis of amplifier IC4 and

20 hence the whole circuit will oscillate at a frequency defined by the expression:-

$$F = I/2Ct[R6/R6+R7][(+VS)-(-VS)]$$

The frequency will consequently be inversely proportional

to the capacitance Ct.

The above capacitance to frequency converter is particularly suitable for use with a displacement capacitive device, in which a pair of plates are mounted

05 such that one plate is connected to the input of the capacitance to frequency converter and the other is spaced a small distance away and connected to the zero voltage supply (OVS). A small capacitance will now exist between the two plates, typically 1-2 pF. The plate connected to

10 the zero voltage supply (OVS) can be made to move relative to the other plate when for example subjected to load or pressure.

The buffer amplifier or capacitance to frequency converter described above may be made from discrete components or may

15 themselves be in the form of integrated circuits. If an integrated circuit capacitance to frequency converter is used in a displacement capacitive device of the form disclosed above, one of the plates may itself be built on to the surface of the integrated circuit to form a

20 monolithic component. The other plate of the displacement capacitive device may then be provided by a conductive element which is deformable under a load applied thereto. This element may, for example, be the wall of a casing of a load cell or pressure transducer.

CLAIMS

1.   An amplifier comprising a first integrated circuit differential amplifier, the output of the differential amplifier being fed back to its inverting input, an input being applied to its non-inverting input and means being

05   provided in the positive and negative supply lines by which the input signal to the differential amplifier may be imposed on the positive and negative supplies.

2.   An amplifier according to Claim 1 in which the output of said first differential amplifier is connected to

10   the non-inverting inputs of a second and third differential amplifier, the inverting input of said second differential amplifier being connected to the negative voltage source and its output being connected to the positive voltage supply of said first differential amplifier and the

15   inverting input of said third differential amplifier being connected to the positive voltage source and its output being connected to the negative voltage supply of the first differential amplifier.

20 3.   An amplifier according to Claim 2 in which the inverting input of the second differential amplifier is

connected to its output via a first zener diode and the
inverting input of the third differential amplifier is
connected to its output via a second zener diode, the sum
of the reference voltages of the zener diodes being equal
05   to the supply voltage applied across the first differential
amplifier.

4.   An amplifier according to any one of Claims 1 to 3
in which the inverting input of the first differential
amplifier is connected to a screen of the lead applying the
10   input signal to the non-inverting input.

5.   An amplifier substantially as described herein
with reference to and as shown in Figure 1 of the
accompanying drawings.

6.   A capacitance to frequency converter comprising an
15   amplifier as claimed in any one of Claims 1 to 5, the
output of the first differential amplifier being connected
to the inverting input of a further integrated circuit
differential amplifier, the further differential amplifier
being configured as a Schmitt Trigger, common positive and
20   negative voltage supplies being applied across the first
and second differential amplifiers.

7.   A capacitance to frequency converter according to

Claim 6 in which the output of the further differential amplifier is connected to; the non-inverting input of the first differential amplifier via first and second resistances, its inverting input via the first and a third resistance and its non-inverting input via a fourth resistance; and the non-inverting input of the further differential amplifier is connected to a zero voltage supply via a fifth resistance.

8.   A capacitance to frequency converter substantially as described herein with reference to and as shown in Figure 2 of the accompanying drawings.

9.   An electronic circuit according to any one of Claims 1 to 8 formed as an integrated circuit.

10.   A displacement capacitance device comprising a pair of plates mounted so that one is movable relative to the other and a capacitance to frequency converter as described in any one of Claims 6 to 9.

11.   A displacement capacitance device according to Claim 10 when taken with Claim 9, in which one of said plates is built on to the surface of the integrated circuit to form a monolithic component.