**IC 4017** is the **5 stage Johnson Decade counter** IC widely used in chaser lighting circuits. It takes the clock pulses from the **Clock input** and makes one of the ten outputs On in sequence each time a Clock pulse arrives. A **Johnson counter,** also called **Walking ring counter** is the modified Ring counter in which the last stage is Inverted and fed back as the input to the first stage. It is a **Decade counter** since the counting is in **Decimal digits** and not in **Binary**. See the working details of CD 4017 and the Circuits.



**CD 4017** or **HEF 4017** are 16 pin **CMOS** version ICs belonging to the **4000 series**. Internally the IC has **5 Bistables** which are interconnected in the**Johnson counter** pattern. The outputs of the Bistables are **decoded** to give **10 individual outputs**.The IC, take clock pulse from an **external oscillator** and steps the outputs from negative to positive in a series of 10 steps. *Only one output will be high at a time.* The IC can be exploited in different ways. It can be used to count up to a certain number and repeating the sequence or halting the count after a particular count or it can be cascaded to another 4017 IC to get higher numbers. It can be also used as a Bistable latch in the toggle mode.

**CD 4017** works off **5-15 volts** while **HEF 4017** operates  from **3 volts**. It has 10 outputs and each output can sink **10 mA** current.

It works based on the **Johnson counter method** in which the *last stage in inverted and fed to the first stage as input*. It is also known as **Switch tail ring counter,** **Twisted ring counter** or **Moebius counter.** The **Register** of the IC cycles through a sequence of**Bit patterns**. The*length of the bit pattern is equal to twice the length of the Shift register.* The Register cycles continue infinitely. Johnson counter has **2n output states** where the **n** is the number of **Flip-Flops** in the chain. It is a **Decade counter** that makes the counts in **Digits.** It is also known as **Mod counter** when it counts to 10 from 0 to 1, 2, 3 etc. *A****Mod counter****that counts to 10 stops at 9 because the 0 count is a valid count.*

The IC has **10 Spike free Decoded outputs Q0 to Q9,** an**Active low Carry out pin** and **Active high and Active low inputs** namely **CP0** and **CP1**.Its **Reset pin** is an **Overriding Asynchronous Master Reset( MR)**. T*he counter advances by either a Low – to – High transition pulse at Active high input CP0 while CP1 is low or a High – to – Low transition at Active low input CP1 when CP0 is high.* A **High pulse**at the **Master Reset** pin will resets the counter to 0 independent of the clock pulses at CP0 or CP1. The IC also has an **Automatic counter code correction** mechanism. If there is an illegal code, the counter will returns to the normal counting mode with in 11 clock pulses. The **Clock inputs** are highly sensitive ( Even the e.m.f around the live wire can clock the inputs) and tolerant to slower rise and fall times.

**Pin connection**



1. – 6th sequential output
2. -2nd sequential output
3. – 1st sequential output
4. -3rd sequential output
5. – 7th sequential output
6. – 8th sequential output
7.- 4th sequential output
8. Ground
9 – .9th sequential output
10.- 5th sequential output
11. – 10th sequential output
12. CO – Carry Out – Outputs high on counts 0 to 4. Outputs low on counts 5 to 9 .Thus a transition from low to high occurs when counting from 9 back to 0)

13. LE – Latch Enable – latches on the current output when high (i.e. the chip counts when LE is low)
14. CLK – Clock In
15. RST – Reset – Sets output 1 high and outputs 2 through 10 low, when taken high
16.Vcc – + 3 to +15 Volts DC.