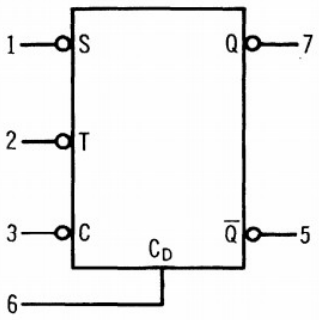
MC974 • MC874

Available in TO-99 metal can, add "G" suffix.

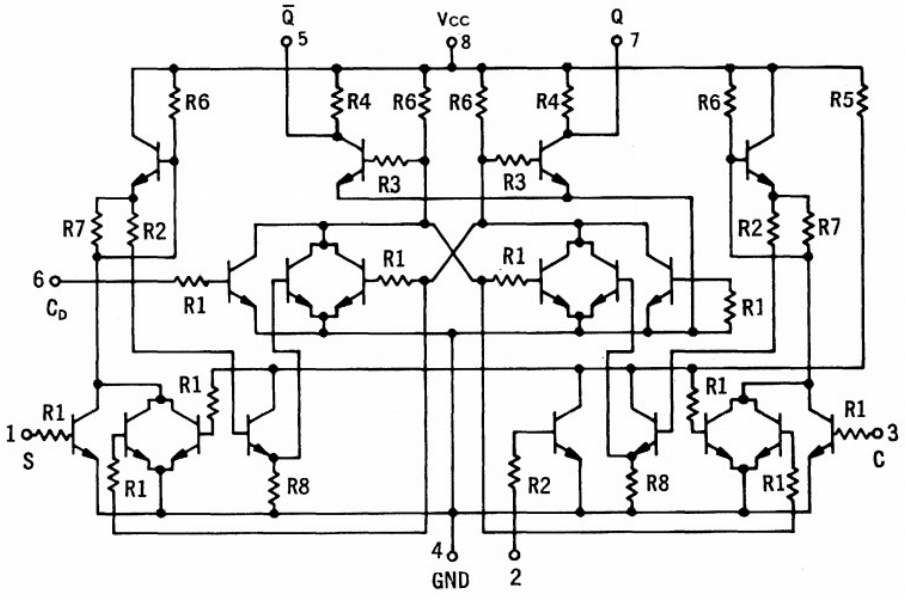
J-K flip-flop with a direct clear input
in addition to the clocked inputs.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 700 Ω
R2 = 300 Ω	R6 = 900 Ω
R3 = 550 Ω	R7 = 2k Ω
R4 = 640 Ω	R8 = 3k Ω

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC974	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC874	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC974 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC874 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	6	-	8	4
	$2\ I_{in}$*	2	-	990	-	870	-	940		-	1008	-	900	-	900		2	-	1,3	-		
	I_{in}	3 Δ	-	495	-	435	-	470		-	504	-	450	-	450		3	-	-	-		
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	-	-		
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5,6	-	-	8	4
		7 Δ	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7	-	-	8	4
Saturation Voltage	$V_{CE(sat)}$	5‡§	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	3	8	4
		5‡§	-		-		-			-		-		-			-	-	-	1,3		
		5Δ§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ	-		-		-			-		-		-			-	6	-	-		
		7‡§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ§	-		-		-			-		-		-			-	3	-	1		
		7Δ§	-		-		-			-		-		-			-	-	-	1,3		

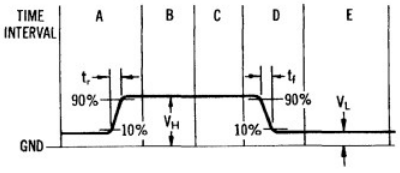
Pins not listed are left open.

Δ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 6 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 6, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note §) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 1 and 3, and proceed with the test.

‡ Momentarily apply V_{BOT} to pin 6 prior to the arrival of the negative-going clock pulse to effect a change of state.

§ Clock Pulse to pin 2:

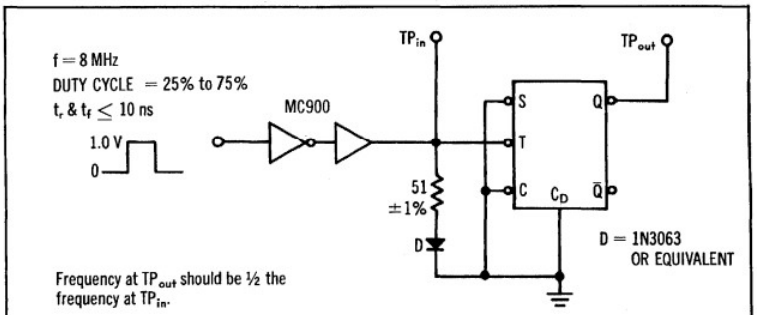
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC874		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC974		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

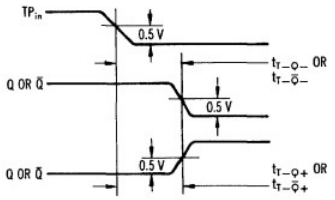
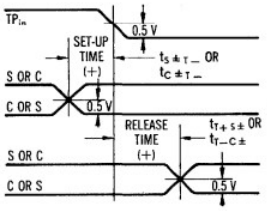
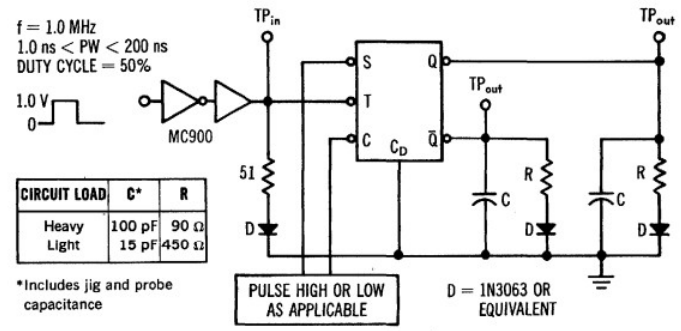


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

*Includes jig and probe capacitance

SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
t_{C_D+Q-}	4	—	90
$t_{C_D+\bar{Q}+}$	4	—	70

Lightly loaded * Negative switching time means the inputs can momentarily change before the clock pulse transition.

FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME