T-49-19-08

Microchip

# PIC1654S

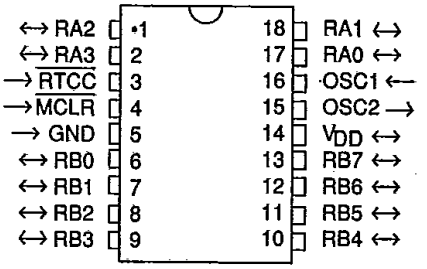
## 8-Bit Microcontroller

### FEATURES

- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self contained oscillator for crystal or ceramic resonator
- Access to RAM registers inherent to instruction
- Available in three temperature ranges: 0° to 70°C, -40° to 85°C and -40° to 110°C
- 18 pin package
- 2 level stack for subroutine nesting
- Open drain option on all I/O lines
- 12 bi-directional I/O lines
- 2 µsec instruction execution time

**PIN CONFIGURATION**
18 Lead Dual In Line
18 Lead SOIC

**Top View**




### DESCRIPTION

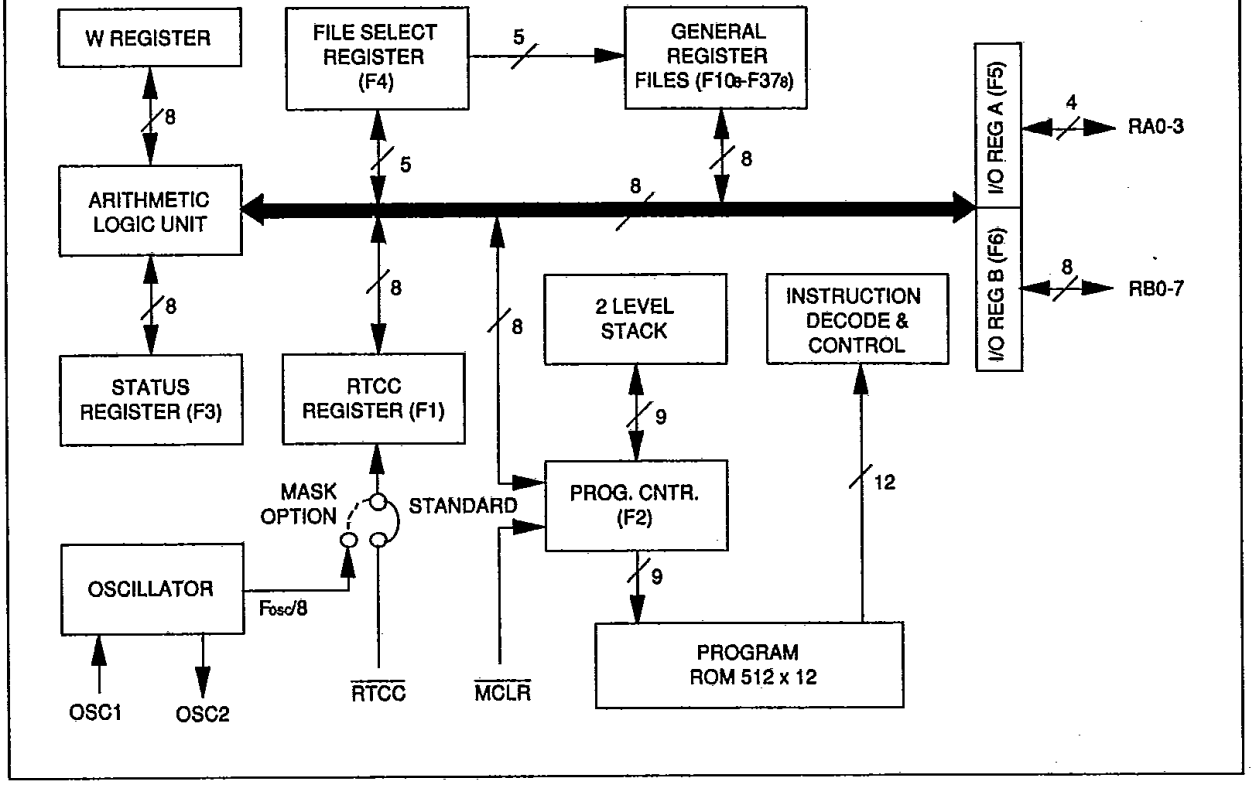
The PIC1654S microcontroller is a MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities for motor control, telecommunication equipment, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1654S is fabricated with N-Channel Silicon Gate technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal or ceramic resonator to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALC, a powerful macroassembler. PICALC is available in various versions that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PICES II real time In-Circuit Emulation System, PIC Field Demo boards (PFD), and the ROM-less version of the PIC1654S, the PIC1664, provide all required development and debugging tools.

**PIC1654S BLOCK DIAGRAM**




## ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcontroller is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock/Counter (RTCC), the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777₈.

**PIN FUNCTION TABLE**

| Signal | Definition |
|---|---|
| OSC1 (Input), OSC2 (Output) | These pins are the time base inputs to which a crystal, ceramic resonator, or external single phase clock may be connected. The frequency of oscillation is 8 times the instruction cycle frequency. |
| $\overline{\text{RTCC}}$ (Input) | Real Time Clock/Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock/Counter Register increments on falling edges applied to this pin. This register (F1) can be loaded and read by the program. This is a Schmitt trigger input. A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock counter register. In this mode, transitions in the $\overline{\text{RTCC}}$ pin will be disregarded. However, the pin must be tied to either Vss or VDD to avoid unintended test mode activation. |
| RA0-3 (Input/Output) | 4 user programmable I/O lines (F5). The four MSB's are always read as logic 0's. All inputs and outputs are under direct control of the program. A mask option will allow any I/O pin at the time of ROM pattern definition to be open drain. |
| RB0-7 (Input/Output) | 8 user programmable I/O lines (F6).<br>All inputs and outputs are under direct control of the program. A mask option will allow any I/O pin at the time of ROM pattern definition to be open drain. |
| $\overline{\text{MCLR}}$ (Input) | Master Clear. Used to initialize the internal ROM program to address $777_8$ and latch all I/O registers high. Should be held low 10 - 75ms past the time when $V_{DD} \geq 4.5V$ depending on the crystal start up time.<br>This is a Schmitt trigger input. |
| VDD | Power supply. |
| Vss | Ground pin. |

## REGISTER FILE ARRANGEMENT

| File (Octal) | Function |
|---|---|
| F0 | Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W + F0 → W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W. |
| F1 | Real Time Clock/Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on high-to-low transitions on the RTCC input. However, if data is being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer. |
| F2 | Program Counter (PC). The nine bit wide PC is automatically incremented during each instruction cycle, unless it is written into under program control (MOVWF F2, GOTO, CALL, ADDWF F2, RETLW). CALL, MOVWF2, ADDWF2 instructions write only the 8 low order bits of the PC, while the MSB is made to zero. Only the 8 low order bits of F2 can be read under program control. |
| F3 | Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.<br>(7) (6) (5) (4) (3) (2) (1) (0)<br>1 1 1 1 1 Z DC C<br>C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.<br>DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant. Note that a subtraction os always executed as an addition of the two's complement of the second operand.<br>Z (Zero): Set if the result of an Arithmetic operation is zero.<br>Bits: 3-7 These bits are defined as logic ones. |
| F4 | File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones. |
| F5 | I/O Register A (RA0-RA3) (RA4 - RA7 defined as zeros). |
| F6 | I/O Register B (RB0-RB7). |
| F7-F37$_8$ | General Purpose Registers. |

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## BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code that specifies the instruction type and one or more operands specifying the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit oriented instructions, "b" represents a bit field designator that selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight- or nine-bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time is 2 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction*. In these two cases, the instruction execution time is 4 μsec.

* (GOTO, CALL, RETLW, MOVWF2, ADDWF2).

**BYTE-ORIENTED FILE REGISTER**

For d = 0, f → W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f → f (if d is omitted, assembler assigns d = 1).

| (11-6) | (5) | (4-0) |
|---|---|---|
| OP CODE | d | f(FILE #) |

| Instruction-Binary (Octal) | | | | | Name | Mnemonic, Operands | | Operation | Status Affected |
|---|---|---|---|---|---|---|---|---|---|
| 000 | 000 | 000 | 000 | (0000) | No Operation | NOP | - | - | None |
| 000 | 000 | 1ff | fff | (0040) | Move W to f (Note 1) | MOVWF | - | W→f | None |
| 000 | 001 | 000 | 000 | (0100) | Clear W | CLRW | - | 0→W | Z |
| 000 | 001 | 1ff | fff | (0140) | Clear f | CLRF | f | 0→f | Z |
| 000 | 010 | dff | fff | (0200) | Subtract W from f | SUBWF | f,d | f-W→d [f + $\overline{W}$ + 1→d] | C,DC,Z |
| 000 | 011 | dff | fff | (0300) | Decrement f | DECF | f,d | f-1→d | Z |
| 000 | 100 | dff | fff | (0400) | Inclusive OR W and f | IORWF | f,d | W∨f→d | Z |
| 000 | 101 | dff | fff | (0500) | ANDbW and f | ANDWF | f,d | W•f→d | Z |
| 000 | 110 | dff | fff | (0600) | Exclusive OR W and f | XORWF | f,d | W⊕f→d | Z |
| 000 | 111 | dff | fff | (0700) | Add W and f | ADDWF | f,d | W + F→d | C,DC,Z |
| 001 | 000 | dff | fff | (1000) | Move f | MOVF | f,d | f→d | Z |
| 001 | 001 | dff | fff | (1100) | Complement f | COMF | f,d | f→d | Z |
| 001 | 011 | dff | fff | (1200) | Increment f | INCF | f,d | f + 1→d | Z |
| 001 | 011 | dff | fff | (1300) | Decrement f, Skip to Zero | DECFSZ | f,d | f - 1→d, skip if Zero | None |
| 001 | 100 | dff | fff | (1400) | Rotate Right f | RRF | f,d | f(n)→d(n-1), C→d(7), f(0)→C | C |
| 001 | 101 | dff | fff | (1500) | Rotate Left f | RLF | f,d | f(n)→d(n + 1), C→d(0), f(7)→C | C |
| 001 | 110 | dff | fff | (1600) | Swap halves f | SWAPF | f,d | f(0-3)↔f(4-7)→d | None |
| 001 | 111 | dff | fff | (1700) | Increment f, Skip if Zero | INCFSZ | f,d | f + 1→d, skip if Zero | None |

**BIT-ORIENTED FILE REGISTER OPERATIONS**

| (11-8) | (7-5) | (4-0) |
|---|---|---|
| OP CODE | b (BIT #) | f(FILE #) |

| Instruction-Binary (Octal) | | | | | Name | Mnemonic, Operands | | Operation | Status Affected |
|---|---|---|---|---|---|---|---|---|---|
| 010 | 0bb | bff | fff | (2000) | Bit Clear f | BCF | f,b | 0→f(b) | None |
| 010 | 1bb | bff | fff | (2400) | Bit Set f | BSF | f,b | 1→f(b) | None |
| 011 | 0bb | bff | fff | (3000) | Bit Test f, skip if Clear | BTFSC | f,b | Bit Test f(b): skip if clear | None |
| 011 | 1bb | bff | fff | (3400) | Bit Test f, skip if Set | BTFSS | f,b | Bit Test f(b): skip if set | None |

**LITERAL AND CONTROL OPERATIONS**

| (11-8) | (7-0) |
|---|---|
| OP CODE | k (LITERAL) |

| Instruction-Binary (Octal) | | | | | Name | Mnemonic, Operands | | Operation | Status Affected |
|---|---|---|---|---|---|---|---|---|---|
| 100 | 0kk | kkk | kkk | (4000) | Return and place Literal in W | RETLW | k | k→w, Stack→PC | None |
| 100 | 1kk | kkk | kkk | (4400) | Call subroutine (Note 1) | CALL | k | PC+1-Stack, k→PC | None |
| 101 | kkk | kkk | kkk | (5000) | Go to address (k is 9 bits) | GOTO | k | k→PC | None |
| 110 | 0kk | kkk | kkk | (6000) | Move Literal to W | MOVLW | k | k→W | None |
| 110 | 1kk | kkk | kkk | (6400) | Inclusive OR Literal and W | IORLW | k | kVW→W | Z |
| 111 | 0kk | kkk | kkk | (7000) | AND Literal and W | ANDLW | k | k•W→W | Z |
| 111 | 1kk | kkk | kkk | (7400) | Exclusive OR Literal and W | XORLW | k | k⊕W→W | Z |

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377ₒ. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

 

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## SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3.0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

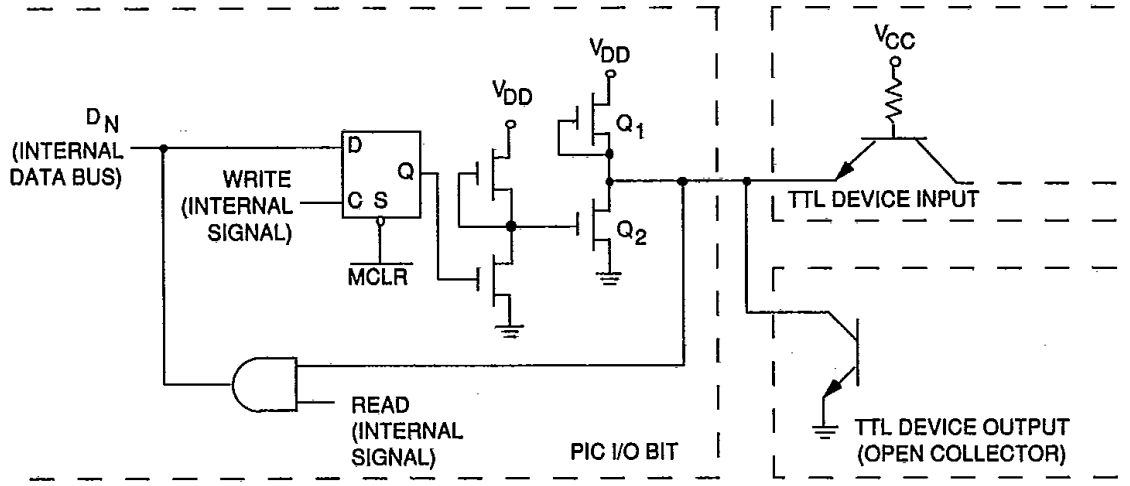
**SUPPLEMENTAL INSTRUCTION SET SUMMARY**

| Instruction-Binary (Octal) | | | | | Name | Mnemonic, Operands | Operation | Status Affected |
|---|---|---|---|---|---|---|---|---|
| 010 | 000 | 000 | 011 | (2003) | Clear Carry | CLRC | BCF 3, 0 | - |
| 010 | 100 | 000 | 011 | (2403) | Set Carry | SETC | BSF 3, 0 | - |
| 010 | 000 | 100 | 011 | (2043) | Clear Digit Carry | CLRDC | BCF 3, 1 | - |
| 010 | 100 | 100 | 011 | (2443) | Set Digit Carry | SETDC | BSF 3, 1 | - |
| 010 | 001 | 000 | 011 | (2103) | Clear Zero | CLRZ | BCF 3, 2 | - |
| 010 | 101 | 000 | 011 | (2503) | Set Zero | SETZ | BSF 3, 2 | - |
| 011 | 100 | 000 | 011 | (3403) | Skip on Carry | SKPC | BTFSS 3, 0 | - |
| 011 | 000 | 000 | 011 | (3003) | Skip on No Carry | SKPNC | BTFSC3, 0 | - |
| 011 | 100 | 100 | 011 | (3443) | Skip on Digit Carry | SKPDC | BTFSS 3, 1 | - |
| 011 | 000 | 100 | 011 | (3043) | Skip on No Digit Carry | SKPNDC | BTFSC 3,1 | - |
| 011 | 101 | 000 | 011 | (3503) | Skip on Zero | SKPZ | BTFSS 3, 2 | - |
| 011 | 001 | 000 | 011 | (3103) | Skip on No Zero | SKPNZ | BTFSC3, 2 | - |
| 001 | 000 | 1ff | fff | (1040) | Test File | TSTF f | MOVF f, 1 | Z |
| 001 | 000 | 0ff | fff | (1000) | Move File to W | MOVFW f | MOVF f, 0 | Z |
| 001 | 001 | 1ff | fff | (1140) | Negate File | NEGF f,d | COMF f, 1 | |
| 001 | 010 | dff | fff | (1200) | | | NCFf,d | Z |
| 011 | 000 | 000 | 011 | (3003) | Add Carry to File | ADDCF f,d | BTFSC 3,0 | |
| 001 | 010 | dff | fff | (1200) | | | INCF f,d | Z |
| 011 | 000 | 000 | 011 | (3003) | Subtract Carry from File | SUBCF f,d | BTFSC 3, 0 | |
| 000 | 011 | dff | fff | (0300) | | | DECF f,d | Z |
| 011 | 000 | 100 | 011 | (3043) | Add Digit Carry to File | ADDDCF f,d | BTFSG 3, 1 | |
| 001 | 010 | dff | fff | (1200) | | | INCF f,d | Z |
| 011 | 000 | 100 | 011 | (3043) | Subtract Digit Carry from File | SUBDCF f,d | BTFSC 3, 1 | |
| 000 | 011 | dff | fff | (0300) | | | DECF f,d | Z |
| 101 | kkk | kkk | kkk | (5000) | Branch | B k | GOTO k | - |
| 011 | 000 | 000 | 011 | (3003) | Branch on Carry | BC k | BTFSC 3, 0 | |
| 101 | kkk | kkk | kkk | (5000) | | | GOTO k | - |
| 011 | 100 | 000 | 011 | (3403) | Branch on No Carry | BNC k | BTFSS 3, 0 | |
| 101 | kkk | kkk | kkk | (5000) | | | GOTO k | - |
| 011 | 100 | 100 | 011 | (3043) | Branch on Digit Carry | BDC k | BTFSC 3, 1 | |
| 101 | kkk | kkk | kkk | (5000) | | | GOTO k | - |
| 011 | 001 | 000 | 011 | (3443) | Branch on No Digit Carry | BNDC k | BTFSS 3, 1 | |
| 101 | kkk | kkk | kkk | (5000) | | | GOTO k | - |
| 011 | 101 | 000 | 011 | (3103) | Branch on Zero | BZ k | BTFSC 3, 2 | |
| 101 | kkk | kkk | kkk | (5000) | | | GOTO k | - |
| 011 | 101 | 000 | 011 | (3503) | Branch on No Zero | BNZ k | BTFSS 3, 2 | |
| 101 | kkk | kkk | kkk | (5000) | | | GOTO k | - |

## I/O INTERFACING

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off $Q_2$, allowing the TTL open collector device to drive the pad, pulled up by $Q_1$, which can source a minimum of 100µA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

**TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE**




NOTE: TRANSISTOR $Q_1$ CAN BE REMOVED PER MASK OPTION TO FORM AN OPEN-DRAIN OUTPUT.

## PROGRAMMING CAUTIONS

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

### BIDIRECTIONAL I/O PORTS

The bidirectional ports may be used for both inut and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output latch must be set in the high state. Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

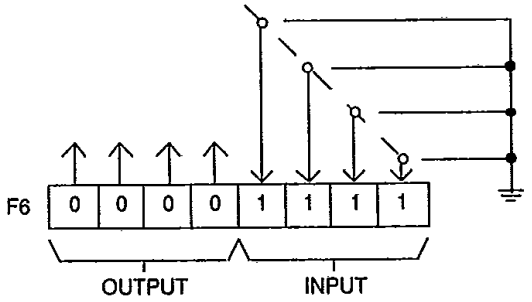
Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F6 (port RB) will cause all eight bits of F6 to be read into the CPU. Then the BSF operation takes place on bit 5 and F6 is re-output to the output latches. If another bit of F6 is used as an inut (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples on the next page.

## Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if tpd (See I/O Timing Diagram) is greater than 1/4tcy (min). When in doubt, it 's better to separate these instructions with a NOP or other instruction.

**EXAMPLE 1**

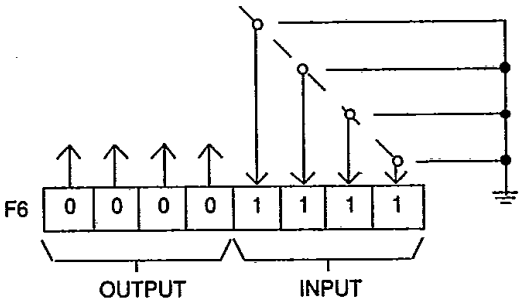



What is thought to be happening:
BSF 6,5

| | |
|---|---|
| Read into CPU: | 00001111 |
| Set bit 5: | 00101111 |
| Write to F6: | 00101111 |

If no inputs were low during the instruction execution, there would be no problem.

**EXAMPLE 2**




What could happen if an input were low:
BSF 6,5

| | |
|---|---|
| Read into CPU: | 00001110 |
| Set bit 5: | 00101110 |
| Write to F6: | 00101110 |

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

## ELECTRICAL CHARACTERISTICS

**Maximum Ratings***

Ambient temperature under bias..... 125°C
Storage Temperature ..... - 55°C to +150°C
Voltage on any pin with respect to Vss (except open drain) ..... -0.3V to + 9.0V
Voltage on any pin with respect to Vss (open drain) ..... -0.3V to + 13V
Power Dissipation (Note 1) ..... 800mW

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

**DC CHARACTERISTICS - PIC16C54S**

Operating temperature $T_A$ = 0°C to + 70°C

| Characteristic | Sym | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | 4.5 | - | 7.0 | V | |
| Primary Supply Current | $I_{DD}$ | - | 30 | 50 | mA | All I/O pins @ $V_{DD}$ (See Primary Supply Current Chart for additional information). |
| Input Low Voltage | $V_{IL}$ | -0.2 | - | 0.8 | V | |
| Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1) | $V_{IH}$ | 2.4 | - | $V_{DD}$ | V | |
| Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC1) | $V_{IH2}$ | $V_{DD}$ - 1 | - | $V_{DD}$ | V | (Note 4) |
| Output High Voltage | $V_{OH}$ | 2.4 | - | $V_{DD}$ | V | $I_{OH}$ = -100µA provided by internal pullups (Note 2) |
| Output Low Voltage (I/O only) | $V_{OL1}$ | - | - | 0.45 | V | $I_{OL}$ = -1.6mA, (Note 3) |
| Input $\overline{RTCC}$ Current | $I_{RTCC}$ | - | 7 | 20 | µA | $V_{SS} \le V_{IN} \le V_{DD}$ |
| Input Leakage Current ($\overline{MCLR}$) | $I_{IC}$ | - 5 | - | + 5 | µA | $V_{SS} \le V_{IN} \le V_{DD}$ |
| Output Leakage Current (open drain pins) | $I_{OL}$ | - | - | 10 | µA | $V_{SS} \le V_{PIN} \le 12V$ |
| Input Low Current (all I/O ports) | $I_{IL}$ | - 0.2 | - | -1.6 | mA | $V_{IL}$ = 0.4V (internal pullup) |
| Input High Current (all I/O ports) | $I_{IH}$ | - 0.1 | -0.4 | - | mA | $V_{IH}$ = 2.4V |

† Typical data is at $T_A$ = 25°C, $V_{DD}$ = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. Positive current indicates current into pin.
   Negative current indicates current out of pin.
3. Total $I_{OL}$ for all output pins must not exceed 175 mA.
4. Instantaneous voltage on the $\overline{RTCC}$ and $\overline{MCLR}$ input must not exceed $V_{DD}$ + 1V otherwise the test mode may be entered. If the $\overline{RTCC}$ pin is not used in an application it must be tied to Vss or $V_{DD}$.

**DC CHARACTERISTICS-PIC1654S-I**

Operating temperature $T_A$ = -40°C to + 85°C

| Characteristic | Sym | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | 4.5 | - | 7.0 | V | |
| Primary Supply Current | $I_{DD}$ | - | 30 | 54 | mA | All I/O pins @ $V_{DD}$ (See Primary Supply Current Chart for additional information). |
| Input Low Voltage | $V_{IL}$ | -0.2 | - | 0.8 | V | |
| Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1) | $V_{IH}$ | 2.4 | - | $V_{DD}$ | V | |
| Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC1) | $V_{IH2}$ | $V_{DD}$ - 1 | - | $V_{DD}$ | V | (Note 4) |
| Output High Voltage | $V_{OH}$ | 2.4 | - | $V_{DD}$ | V | $I_{OH}$ = -100µA provided by internal pullups (Note 2) |
| Output Low Voltage (I/O only) | $V_{OL1}$ | - | - | 0.45 | V | $I_{OL}$ = -1.6mA (Note 3) |
| Input $\overline{RTCC}$ Current | $I_{RTCC}$ | - | 7 | 20 | µA | $V_{SS} \le V_{IN.} \le V_{DD}$ |
| Input Leakage Current ($\overline{MCLR}$) | $I_{LC}$ | - 5 | - | + 5 | µA | $V_{SS} \le V_{IN.} \le V_{DD}$ |
| Output Leakage Current (open drain pins) | $I_{OL}$ | - | - | 10 | µA | $V_{SS} \le V_{PIN} \le 9V$ |
| Input Low Current (all I/O ports) | $I_{IL}$ | - 0.2 | - | -1.6 | mA | $V_{IL}$ = 0.4V(internal pullup) |
| Input High Current (all I/O ports) | $I_{IH}$ | - 0.1 | -0.4 | - | mA | $T_A$ = 0°C to 85°C<br>$V_{IH}$ = 2.4V |

† Typical data is at $T_A$ = 25°C, $V_{DD}$ = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{ILI}) + \Sigma(V_{DD} - V_{OH})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total $I_{OL}$ for all output pins must not exceed 175 mA.
4. Instantaneous voltage on the $\overline{RTCC}$ and $\overline{MCLR}$ input must not exceed $V_{DD}$ + 1V otherwise the test mode may be entered. If the $\overline{RTCC}$ pin is not used in an application, it must be tied to Vss or $V_{DD}$.

**DC CHARACTERISTICS - PIC1654S-H**

Operating temperature $T_A$ = -40°C to + 110°C

| Characteristic | Sym | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | 4.5 | - | 5.5 | V | |
| Primary Supply Current | $I_{DD}$ | - | 35 | 58 | mA | All I/O pins @ $V_{DD}$ (See Primary Supply Current Chart for additional information). |
| Input Low Voltage | $V_{IL}$ | -0.2 | - | 0.8 | V | |
| Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1) | $V_{IH}$ | 2.4 | - | $V_{DD}$ | V | |
| Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC1) | $V_{IH2}$ | $V_{DD}$ - 1 | - | $V_{DD}$ | V | (Note 4) |
| Output High Voltage | $V_{OH}$ | 2.4 | - | $V_{DD}$ | V | $I_{OH}$ = -100µA provided by internal pullups (Note 2) |
| Output Low Voltage (I/O only) | $V_{OL1}$ | - | - | 0.45 | V | $I_{OL}$ = -1.6mA (Note 3) |
| Input $\overline{RTCC}$ Current | $I_{RTCC}$ | - | 7 | 20 | µA | $V_{SS} \le V_{IN} \le V_{DD}$ |
| Input Leakage Current ($\overline{MCLR}$) | $I_{LC}$ | - 5 | - | + 5 | µA | $V_{SS} \le V_{IN} \le V_{DD}$ |
| Output Leakage Current (open drain I/O pins) | $I_{OL}$ | - | - | 20 | µA | $V_{SS} \le V_{PIN} \le 9V$ |
| Input Low Current (all I/O ports) | $I_{IL}$ | - 0.2 | - | -1.6 | mA | $V_{IL}$ = 0.4V(internal pullup) $T_A$ = 0°C to 110°C |
| Input High Current (all I/O ports) | $I_{IH}$ | - 0.1 | -0.4 | - | mA | $V_{IH}$ = 2.4V |

† Typical data is at $T_A$ = 25°C, $V_{DD}$ = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{ILI}) + \Sigma(V_{DD} - V_{OH})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total $I_{OL}$ for all output pins must not exceed 17 5mA.
4. Instantaneous voltage on the $\overline{RTCC}$ and $\overline{MCLR}$ input must not exceed $V_{DD}$ + 1V otherwise the test mode may be entered. If the $\overline{RTCC}$ pin is not used in an application, it must be tied to $V_{SS}$ or $V_{DD}$.

## AC CHARACTERISTICS - PIC1654S

Operating temperature $T_A$ = 0°C to + 70°C
-40°C to +85°C and -40°C to + 110°C

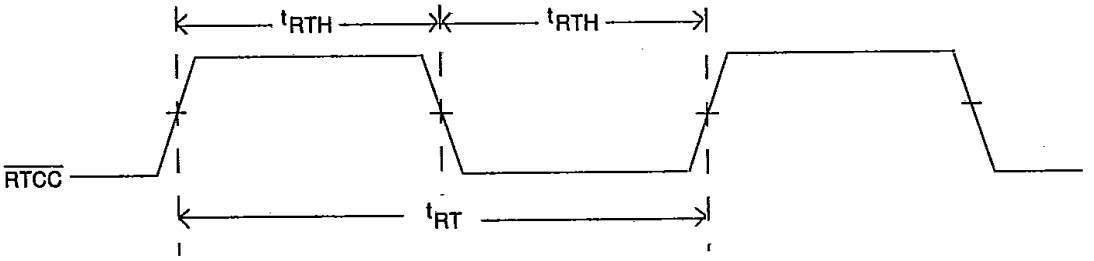
| Characteristic | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Instruction Cycle Time | tCY | 2 | - | 10 | µs | 0.8 MHz - 4.0MHz external time base (Notes 1 and 2) |
| $\overline{\text{RTCC}}$ Input | | | | | | |
| Period | tRT | tCY = 0.2µs- | - | - | - | Note 3 |
| High Pulse Width | tRTH | 1/2 tRT | - | - | - | |
| Low Pulse Width | tRTL | 1/2 tRT | - | - | - | |

NOTES:
1. Instruction cycle period (tCY) equals eights times the input oscillator time base period.
2. The oscillator frequency may deviate to 4.08MHz to allow for tolerance of a crystal or ceramic resonator time base element.
3. The maximum frequency which may be input to the $\overline{\text{RTCC}}$ pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

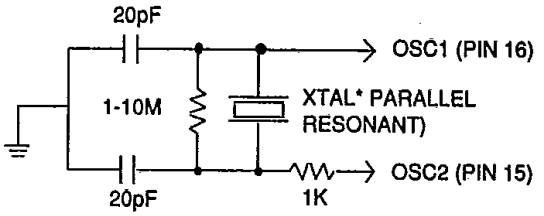
For example: if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

### RTCC TIMING



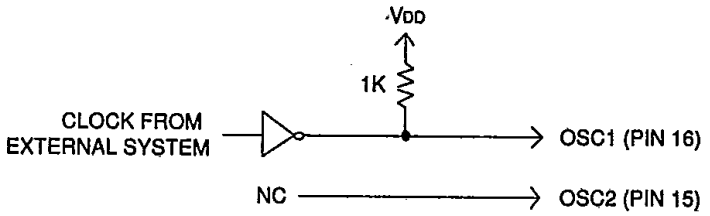
### OSCILLATOR OPTIONS (TYPICAL CIRCUITS) (Cont.)

#### CRYSTAL INPUT OPERATION




* Or ceramic resonator

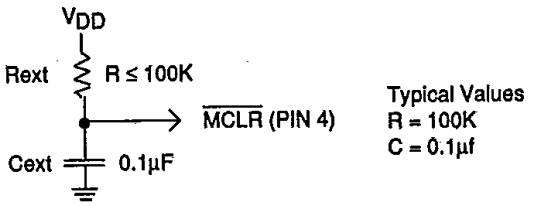
#### EXTERNAL CLOCK INPUT OPERATION




### PRIMARY SUPPLY CURRENT AT SELECTED TEMPERATURES

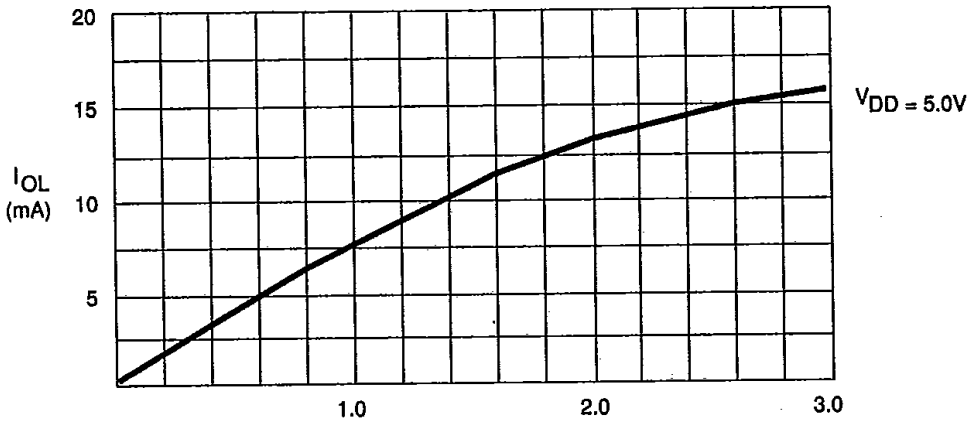
| | | PIC1654S PIC1654S-I | | PIC1654S-H | | | |
|---|---|---|---|---|---|---|---|
| **Characteristic** | **Sym** | **Typ** | **Max** | **Typ** | **Max** | **Units** | **Conditions** |
| Primary Supply Current | IDD | 40 | 54 | 48 | 58 | mA | -40°C, All I/O pins at VDD |
| | | 35 | 50 | 44 | 54 | mA | 0°C, All I/O pins at VDD |
| | | 24 | 45 | 39 | 49 | mA | 70°C, All I/O pins at VDD |
| | | 22 | 42 | 36 | 46 | mA | 85°C, All I/O pins at VDD |
| | | - | - | 30 | 40 | mA | 110°C, All I/O pins at VDD |

## MASTER CLEAR (TYPICAL CIRCUIT)




The $\overline{MCLR}$ pin must be pulsed low for a minimum of one complete instruction cycle ($t_{CY}$) for the master clear function to be guaranteed, assuming that power is applied and the oscillator is running. For initial power application, a delay is required for the external oscillator time base element to start up before $\overline{MCLR}$ is brought high. To achieve this, an external RC configuration, as shown, can be used. This provides approximately a 10ms delay (assuming $V_{DD}$ is applied as a step function), which may be insufficient for some time base elements. Consult the manufacturer of the time base element for the specific start-up times.

## OUTPUT SINK CURRENT GRAPH (TYPICAL)




$I_{OL}$ VS $V_{OL}$

$T_A = 25°C$, $V_{DD} = 5.0V$

## SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

### PART NUMBERS

**PIC1654S - H /P X**

| | | |
|---|---|---|
| **Pattern** | 3-Digit | Pattern Code |
| **Package** | P | Plastic DIP |
| | *SO | SOIC (Gull Wing Lead) |
| | *L | PLCC (J Lead) |
| **Temperature Range** | Blank | 0°C to +70°C |
| | I | -40°C to +85°C |
| | H | -40°C to +110°C |
| **Device** | PIC1654S | |

Notes: *SOIC and PLCC available in Commercial Temperature (0°C to +70°C) only