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AN4104

Forward Converter Type PC SMPS with SPS

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Introduction

The purpose of this application note is to examine basic circuit characteristics, transformer and secondary inductor design methods according to the circuit design, auxiliary power supply terminal and optimum remote control circuit etc., based on the forward converter with SPS (Fairchild power switch) as all related to the desk-top PC SMPS.

First of all, the basic concept of the SPS is to combine the existing MOSFET and its control IC, which were previously separately configured, into 1 package and to include external circuits for configuring existing, various protection features in the internal control IC to execute self-protection. By doing this, the SMPS can be easily designed with few components, enhancing set reliability and production and reducing field defects. These additional effects result in Total cost down, the ultimate purpose to its development.

Various line-up of SPS supports everything from products for 5W auxiliary power supply product to 250W, large capacity SMPS, depending on the type of the internal MOSFET. Table 1 shows the SPS product groups which can be applied to a 220V-input forward converter with different output power.

Because the forward converter has high energy transfer efficiency as compared to the flyback converter, it can obtain a large output using a relatively small transformer and has superior output ripple noise characteristics. For these reasons, it is frequently used in above -150W PC SMPS. Unlike the flyback-type, the forward converter operates with the ON-ON method immediately delivering energy to the secondary side when the transformer primary main switch turns on.

The next section describes the basic circuit operation of this type of forward converter

Table 1.

Device	Freq.	Power
KA5H0165R	100kHz	10 ~ 20W
KA1M0680	70kHz	90 ~ 150W
KA1H0680	100kHz	
KA1L0880	50kHz	180 ~ 250W
KA1M0880	70kHz	

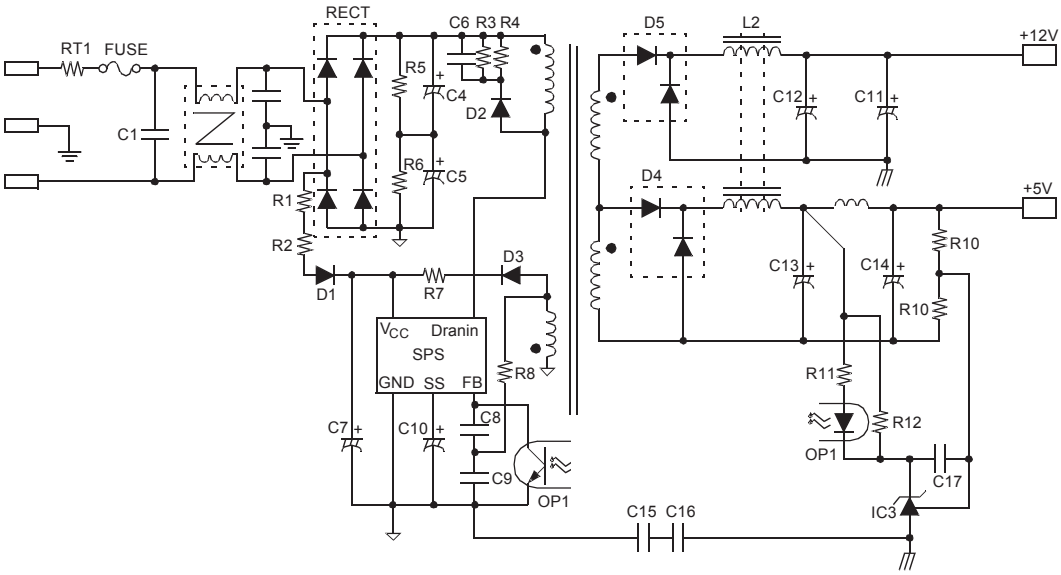


Figure 1. Basic circuit of the Forward converter with SPS

1. FORWARD CONVERTER

1.1 Basic Operation

Figure 2 shows the basic topology of the forward converter. The transformer in the forward converter acts to eliminate the concept of energy storage and acts purely as an energy transfer media. Therefore, the most ideal transformer in the forward converter would be one that has an infinite magnetizing inductor value (Lm) making the circuit an open circuit, essentially. In actuality, however, this magnetizing inductor value is finite. Therefore, a circuit (Figure A) which completely resets the stored energy in the magnetizing inductor before the beginning of the next switching cycle when the switch turns on at every cycle is absolutely needed. Though there are various techniques to form this type of a reset circuit, the transformer reset winding or the RCD clamping circuit etc. is more widely used. It can be said that the forward converter operates basically the same as that of the Buck converter (or also called the Step-down converter). It is just that the desired output voltage can be obtained suitable for off-line by first using the transformer to down the hundreds of DC volts to an appropriate tens of volts and then stepping down through, again, two manual switches (Diode1,2) and the secondary inductor. At this time, D1 always switches the same as the primary main switch (SW) and D2 switches opposite to D1.

The next section reviews the stages along with each waveform of the operation of this type of forward converter.

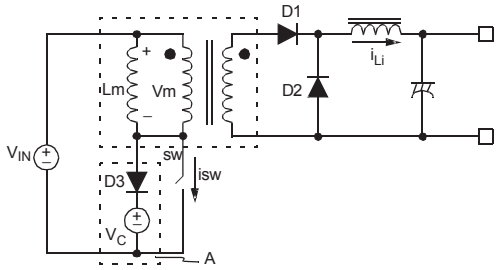


Figure 2. Forward converter topology

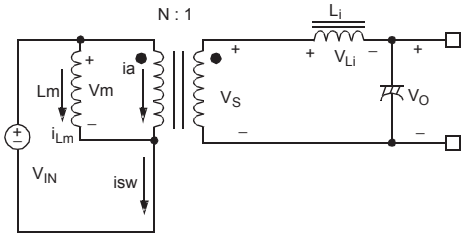


Figure 2a. Equivalent circuit when SW is on (t1~t2)

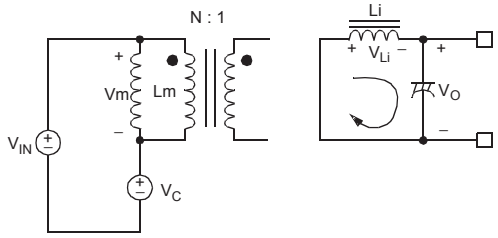


Figure 2b. Equivalent circuit when SW is off (t2~t3)

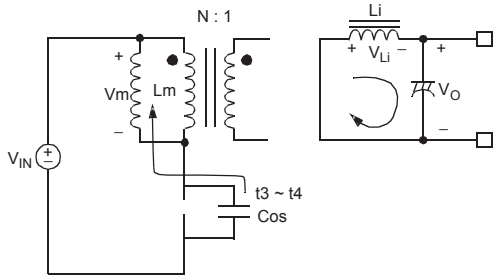


Figure 2c. Equivalent circuit when SW is off (t3~t5)

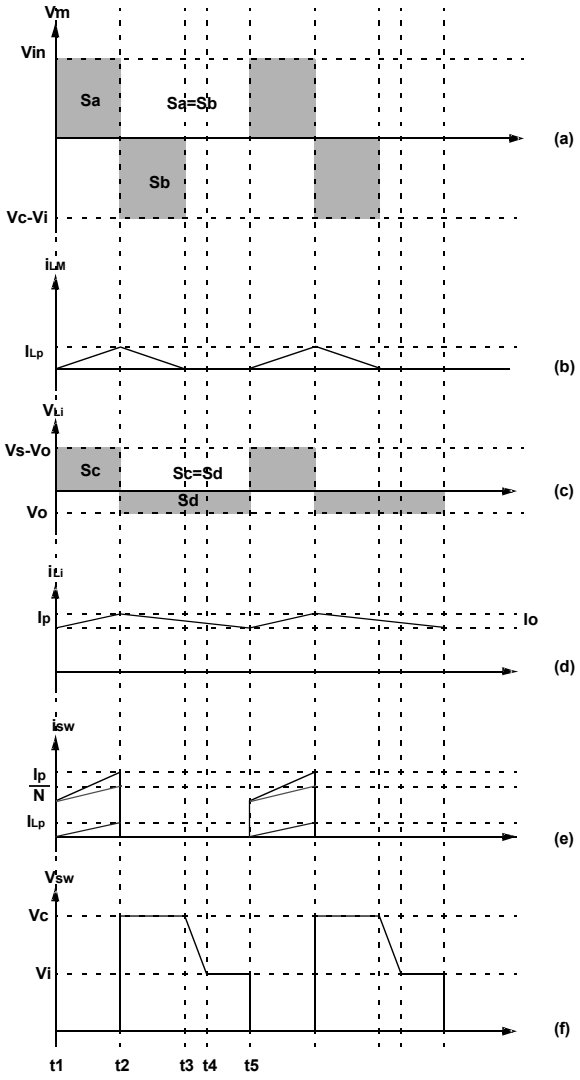


Figure 3. Operating waveform of the forward converter

t1~t2 Interval

Between t1~t2 when the primary side main switch (SW) turns on figure 2 and figure 2a becomes equivalent and the state of each switching element, voltage and current of each terminal can be expressed through the following equations.

SW: on, D1: on, D2: off, D3: off

$Vm = V_{IN}$

$i_{Lm} = (V_{IN} / Lm) \cdot t$

$ia = i_{Li} / N$

$i_{sw} = i_{Lm} + ia = [(V_{IN} / Lm)t] + [i_{Li} / N]$

$V_S = V_{IN} / N$

As revealed above, the current shape of the primary switch in the forward converter is determined by the magnetizing inductance current, i_{Lm}, and the secondary inductor current, i_{Li}.

Looking at figure 2a, voltage Vm equals V_{IN} when the main switch (SW) is on and, in addition, the secondary side voltage, V_S, is applied in one direction, turning on D1. The current delivered through the transformer supplies the output current (Io) through the secondary side inductor (Li). It is stored in Li as magnetic energy until the main switch turns off and then it free wheels through D2 to supply the output current continuously.

t2~t3 Interval

When the primary main switch turns off, reverse voltage is applied to the Vs and D1 turns off. At this time, the energy which was stored in Li during t1~t2 free wheels through D2 to supply output current continuously and D2 turns on. As D3 turns on, the energy stored in the Lm forms the path through which i_{Lm} can continuously flow. At this time, the voltage across Vm is applied with reverse voltage of ($Vc-V_{IN}$) based on Vc making i_{Lm} have a negative slope (Figure 3b) which slowly reduces to become 0 at t3. Consequently, the energy stored in Lm completely resets. Once Vm resets and becomes 0V, D3 turns off.

One item to note here is that the max duty of the forward converter is decided when designing according to the value of Vc. This can be well understood through figure 3(a). As was mentioned previously, D3 and Vc act to completely reset the energy, which was stored in Lm during the interval the SW was on, before the next cycle. For example, if Vc is designed to be $2V_{IN}$, namely, when the Vm reverse voltage is designed to become $-V_{IN}$ when the SW is off and max duty exceeds 50%, the energy stored in Lm does not reset completely before the next cycle and eventually the transformer saturates and the max duty becomes limited to 50%. This is a very important design point for a forward converter and should be especially, carefully considered during designing in order to properly obtain the maximum output under minimum input voltage conditions. The state of each switching element during this internal is as follows:

SW: off, D1: off, D2: on, D3: on

t3~t5 Interval

Once t3 is reached, the stored energy in Lm completely resets; Vm becomes 0V; D3 turns off. The equivalent circuit is shown in figure 2c. The energy stored in the secondary inductor, Li, free wheels through D2 with a slope -Vo / Li until the next main SW turns on and continues to supply output current. [Refer to figures 3c, d]. In this interval, the output voltage determined below is the same as the input/output condition of the Step-down converter

$$V_O = D \times V_S \quad \text{[D: Duty]}$$

$$= D \times (V_{IN} \div N)$$

The voltage waveform of the primary main switch (SW) of the forward converter is a step waveform as in figure 3f. During the interval between t3~t4, there is resonance between the transformer magnetizing inductor (Lm) and the parallel equivalent capacitor of the SW and its voltage decreases to the input voltage.

1.2 Reset Circuit Configuration

The circuit which resets the stored energy in the magnetizing inductor (Lm) in the forward converter, during the time the primary switch is on, is different from Figure 2 and actually configured in the manner shown below.

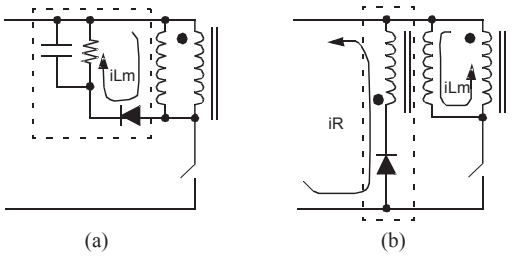


Figure 4. Actual configuration of the reset circuit

As representative reset circuits, figures 4 (a) and (b) have the following characteristics.

Reset Circuit using the RCD

In figure 4(a), the circuit consumes the energy, which was stored in Lm during on time, through the resistor and completely resets the Lm energy before the next cycle. Its concept can be considered the same as that of the RCD snubber circuit, which is used to clamp the flyback leakage inductor's reverse voltage.

The reverse voltage across Lm, which changes with duty, is a special feature of this type of a RCD reset circuit. Even if the input voltage becomes low as the reverse voltage increases due to an increase in duty, it still has beneficial features in normal operation.

Reset Circuit using the Reset Winding

The circuit in figure 4(b) uses a separate reset winding to return the energy stored in Lm to the source to completely reset the energy before the beginning of the next cycle.

When the diode connected in series to the reset winding in figure 4(b) turns on, the voltage across the reset winding equals the input voltage (Vin). Furthermore, a reverse voltage based on the winding ratio of the two windings is applied across Lm and this reverse voltage completely resets the energy. Unlike the concept associated with the above RCD circuit, which consumes the energy stored in Lm, the reset method, which returns the stored energy in Lm to the input using the reset winding, is more advantageous in terms of efficiency. However, if the input voltage decreases, the reverse voltage across Lm decreases and, ultimately, the max duty becomes limited. Therefore, where normal operation is required even at low input voltage, the reset circuit based on the above RCD circuit can be advantageous.

1.3 Coupled Inductor Circuit

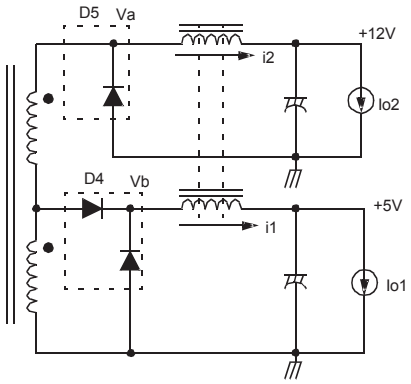


Figure 5. Coupled inductor

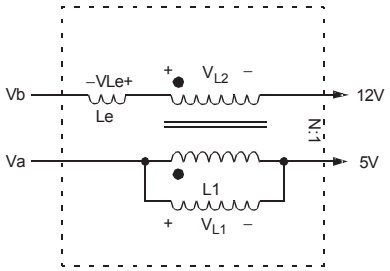


Figure 5.1. Equivalent circuit of the coupled inductor

The output of the forward converter applied in an actual PC SMPS is not simply one but multi-outputs of 3.3V, 5V and ±12V, usually. Among these, the 5V and 12V outputs design the secondary side inductor as a coupled inductor, which uses the same core, as shown in figure 5. The main reason for using the coupled, 5V and 12V inductors is to raise the cross regulation between the two voltages resulting from load fluctuations. If the turn ratio between the two windings and the turn ratio of the transformer do not match when designing this type of coupled inductor, a ripple current increases toward one of the two outputs (Figure 6b/c). This is described well in the equivalent circuit in figure 5.1. If the turn ratio of the coupled inductor is designed well to be 5:12 when the duty is 50%, the transformer turn ratio should be determined such that Va and Vb become 10V and 24V, respectively, for normal operation. However, a case where Vb was designed low such that it only outputs 22V because the transformer turn ratio was not appropriate will be examined.

In such a case, the voltage across L1(V_{L1}) becomes 5V and, accordingly, voltage across L2 (V_{L2}) becomes 12V based on the turn ratio. In addition, the voltage across the leakage inductor has a reverse voltage of -2V and the current shape is such that the ripple voltage at the 5V terminal becomes much larger, as shown by figure 6(c).In order to optimize the ripple current characteristics at the two output terminals, the turn ratio should be determined such that turn ratio of transformer at the two output terminals and the turn ratio of the inductor match. In an actual circuit, this type of turn ratio matching is quite tricky. This is because the diode drop voltage varies according to the amount of output current and because it is difficult to obtain a positive turn ratio.Therefore, an actual design should consider these points such that the output voltage and turn ratio are best matched.

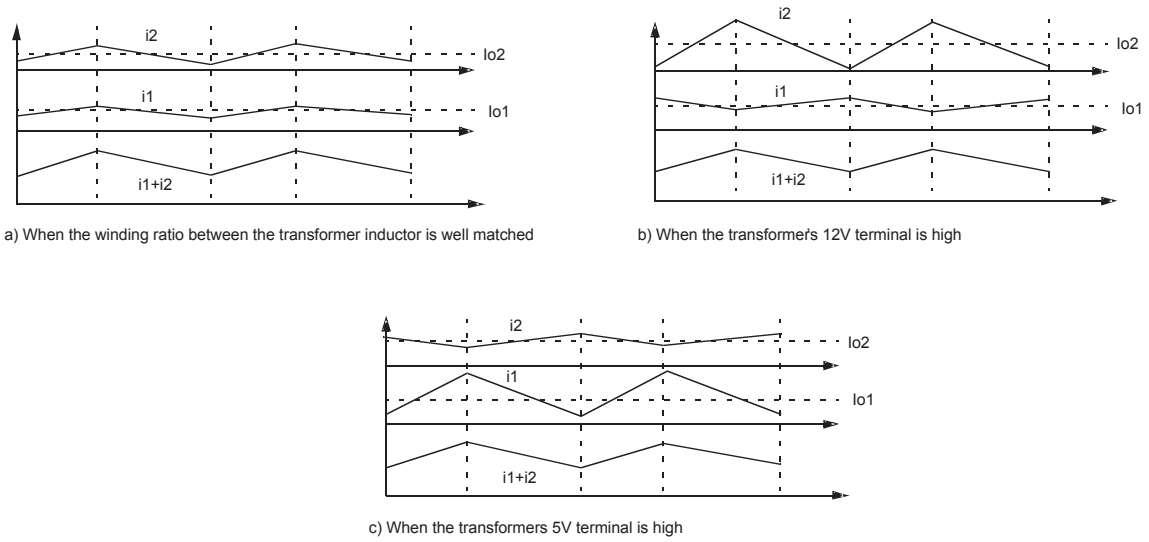


Figure 6. Each waveform of the secondary output terminal

1.4 Hold up Time and Slope Compensation

Like the PC SMPS, a power supply which supplies power to the apparatus which records and saves data requires a minimum hold-up time to safely record the former execution in the event of an instantaneous power failure or off power. The PC SMPS above generally requires this type of hold up time. Once the main power turns off, the energy stored in the DC link capacitor supplies the output power. Furthermore, the input voltage drops as time passes and, therefore, duty must gradually increase in order to supply continuous output power. That is, in order to supply smooth output power when the input voltage drops, the max duty value must be sufficient such that the desired hold - up time is satisfied even when a relatively small input capacitor is used. It must be designed to operate normally up to a fixed duty in order to supply output power over a fixed period of time in the event of an instantaneous power cutoff. Smooth reset must be possible even when the duty increases and input power limitation due to sub-harmonic when duty exceeds 50% in the current mode -controlled PWM SMPS must be prevented. Slope compensation is used to improve the sub-harmonic in this peak current control mode.

Slope Compensation

Sub-harmonic shows cyclic distortion at a frequency lower than the basic switching frequency and, consequently, does not exceed the input power of 50% duty during normal operation. A subharmonic is generated when the duty is above 50% at continuous current mode (CCM) in the peak current control mode. This sub-harmonic is created when the waveforms input to the two PWM comparator inputs do not meet at the point where they are to supposed to coincide. This is because the error amp output of the voltage loop phase lags behind the output voltage waveform.

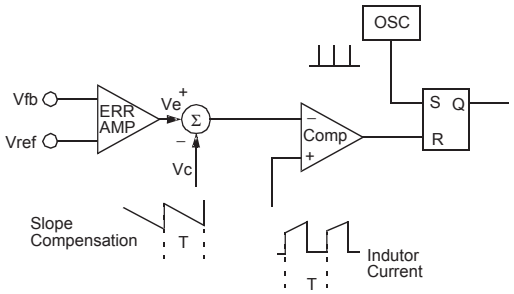


Figure 7. Block diagram of the peak current mode control

Figure 8 shows current waveform distortions according to duty when controlled as an open loop with an ΔIo error. In figure 8a, when the duty is less than 50%, ΔIo converges after few cycles have passed but, in figure 8b, when duty is over 50%, ΔIo gradually gets larger as cycles pass and results in the generation of sub-harmonic oscillation. On the other hand, in figure 8c, even when duty is over 50%, with slope compensation applied at the error amp output, ΔIo converges after few cycles as in figure 8a and, consequently, shows normal operation. Even if duty exceeds 50% due to the lowering of the input voltage, normal output can be supplied without input power limitation from subharmonics by applying slope compensation. Consequently, the desired hold up time requirement can be satisfied even using a small input capacitor. The optimum compensation can be obtained when using 1/2 the negative slope (M2) of the current waveform in figure 2 as the slope, generally, for slope compensation.

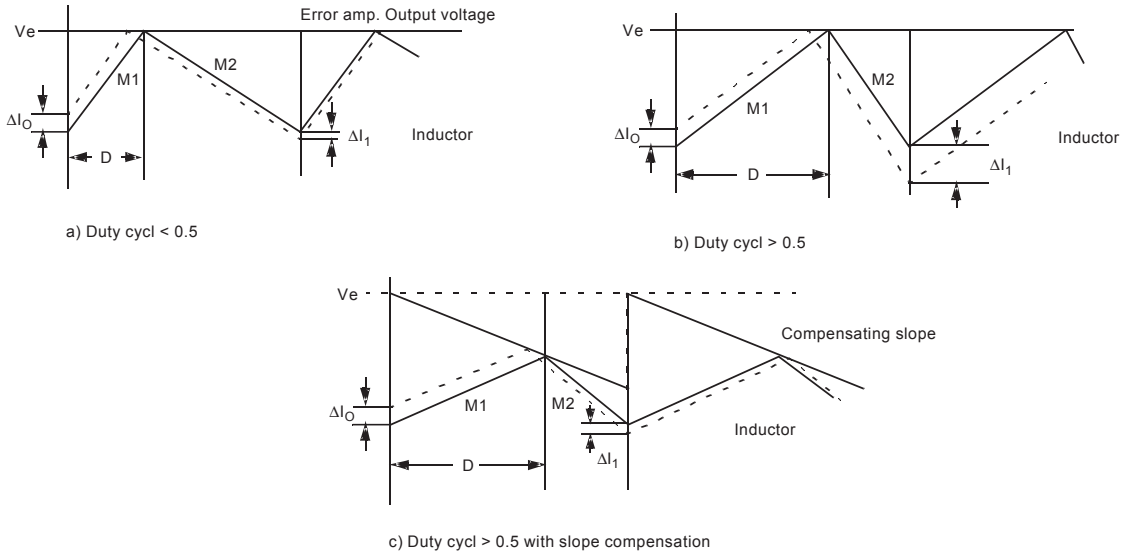


Figure 8. Slope compensation

After having reviewed slope compensation for improving the subharmonic oscillation when controlling through the peak current mode, the application of slope compensation in a circuit with SPS will

be examined. With SPS, the application circuit for slope compensation can be formed more simply than the existing 3842 series, as shown by Figure 9. It can be formed by using the voltage waveform of the V_{CC} terminal winding of the transformer. A negative slope can be obtained when C1 discharges due to the negative voltage at the V_{CC} terminal when the SW is on. This slope is determined by R1 and C1 time constants; the equation is presented below. C1 value should be ten times the C2 value and R1 value can be calculated from equation 1. It can be then designed with the desired slope.

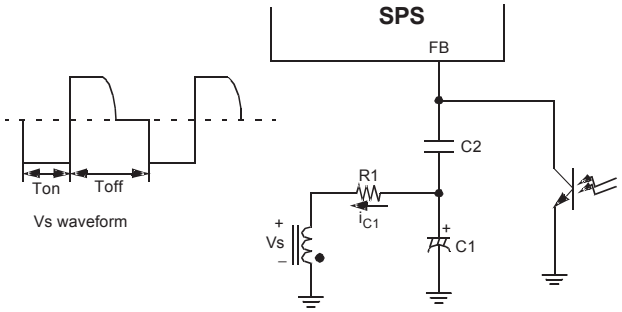
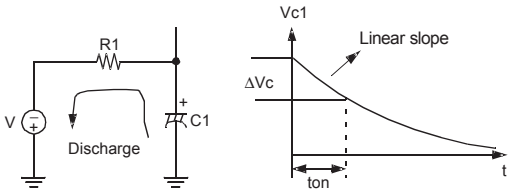


Figure 9. Slope compensation application circuit of the SPS



$$\Delta V_{C1} = V_S(e^{-t_{on}/R_1C_1} - 1) \ldots\ldots\ldots 1$$

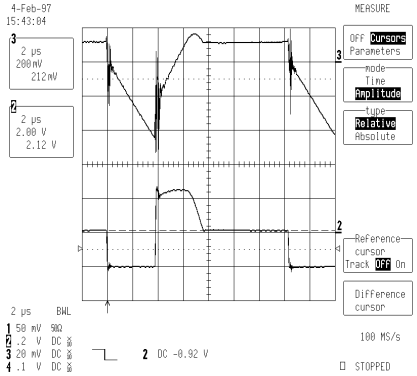


Figure 10. Equivalent circuit of the interval when the SW is ON and FB terminal actual waveform

2. Auxiliary Power Supply

The auxiliary power supply for the PC SMPS requires an output voltage of 5V-10Watt. Unlike the main power supply, this auxiliary power supply is always operating as long as AC input is supplied. The SMPS for the auxiliary power supply is low power -below 10W. It is a circuit with KA1H0165R/ KA1H0165RN flyback configuration using the primary side regulation method to reduce cost.

Figure 11 shows the flyback method auxiliary power supply circuit with KA1H0165R, controlled through primary regulation. The next section reviews each stage of operation of this type of auxiliary power supply terminal.

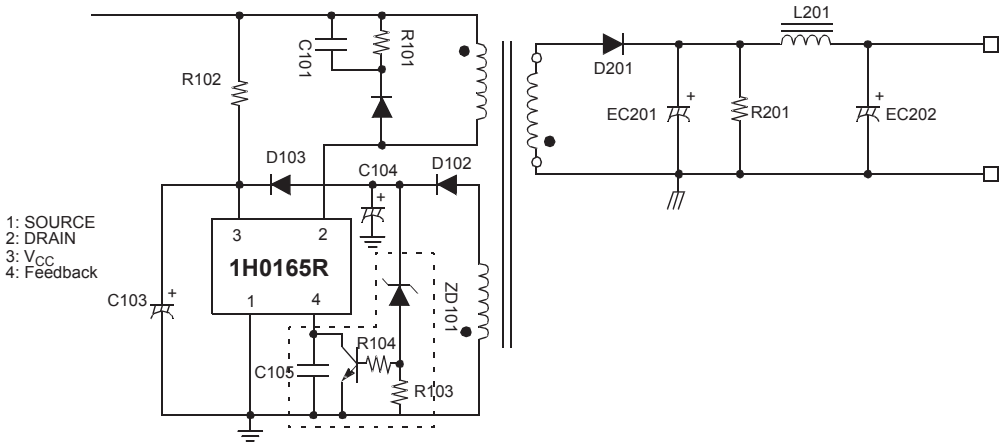


Figure 11. Primary regulation method flyback converter using KA1H0165R

2.1 Start-up

Because the PC SMPS input terminal always uses the voltage doubler, it rectifies with the DC voltage of 220VAC even if 110VAC is input. Therefore, the start up condition for a auxiliary power supply can be calculated based on the 220V input power supply condition flyback design. The start up current consumed in the internal UVLO block before the SPS starts-up is defined to be Max 450μA. Furthermore, the start-up voltage to start internal blocks is 15V and the stop voltage to stop them is 10V.

Furthermore, an appropriate start-up resistance for the auxiliary power supply is calculated such that current over 450μA needed at the start can be supplied to the IC even at the lowest DC input conditions.

The equation is presented below.

$$R102 = (240 - 15) \div 450\mu A = 500k\Omega$$

The time after the AC is input and before the auxiliary power supply starts is determined based on the start-up resistance and capacitance (C103) connected in parallel to the V_{CC} terminal.

2.2 Primary Regulation

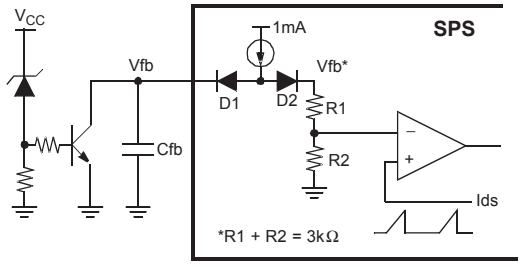


Figure 12. SPS feedback regulation circuit

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Figure 12 shows the block diagram of the SPS internal feedback terminal and the external application circuit used for primary regulation.

When the feedback terminal in the figure is operating normally, Vfb voltage is set to always maintain a fixed V_{CC} voltage and compared to the transformer inductor sensing current (Ids) to determine the PWM duty.

Furthermore, the secondary side output voltage, proportional to the primary side voltage, is based on the transformer turn ratio. To increase the load regulation of the output voltage due to load variations, the coupling coefficient between the primary and secondary side should be designed high when making the transformer and an appropriate dummy resistance attached to the load terminal. The advantage of primary regulation is the cost down effect, but its disadvantage is that precise output voltage regulation is difficult when the load variation is wide.

However, it is useful in a system where the load variation is comparatively stable after power has been applied.

Table 2 shows the parts list of figure 11 needed to form the auxiliary power supply

Table 2. Part list of figure 11

Part	Value	Part	Value
R101	100kΩ	D101	UF4007
R102	500kΩ	D102	1N4937
R103	120Ω	D103	1N4148
R104	1.2kΩ	D201	Shottoky
C101	222 / 630V	C202	470μF / 10V
C103	22μF	R201	470μF / 10V
C103	22μF	R201	500Ω
ZD101	12V / 0.5W	L201	20μH

2.3 Remote ON-OFF Control

The above type of PC SMPS requires a remote control, which can cut off the main power supply terminal operation, through an external or internal signal at stand by. The remote control application circuit for the main power supply terminal with SPS easily controls by “downing” the potentials of the SPS soft-start terminal and the feedback terminal to ground level. The circuit can be formed by adding external components, one TR, one diode and one photocoupler, excluding the existing photo-coupler (OP1) for controlling feedback.

The operation of this remote control can be understood through the SPS internal block in figure 13(b). As shown by the figure, the current source controls the SPS internal feedback terminal. Furthermore, all three, internal diodes are on from 0~3V in the initial state and their voltages are almost equal. Consequently, Vfb, V_{SS} and V_{CO} have the same potentials. Furthermore, if TRs of the photocouplers connected to feedback and soft -start terminals completely saturate in Figure 13

(b), all the current from the current source discharges through the feedback terminal and S/S terminal paths and eventually V_{CO} becomes lower than 0.2V, the transistor saturation voltage. Because the positive terminal of the comparator in figure 13 (b) has a 0.1V offset, the negative terminal of the internal comparator (Comp1) always has a voltage less than the positive terminal if V_{CO} is less than 0.2V and, as a result, the comparator output becomes high state. If the comparator output maintains the high state, the SPS cannot switch any further and cuts off the main power supply terminal operation. Again, to start the main power supply operation, the TR in the secondary side is turned off and OP1 and OP2, which were held back in the primary side, are released. Because the V_{CC} voltage is normal at this time, soft start operation starts like the before and the main power source terminal switches normally. The reason for making the feedback terminal and soft start terminal GND level simultaneously for the remote control is as follows:

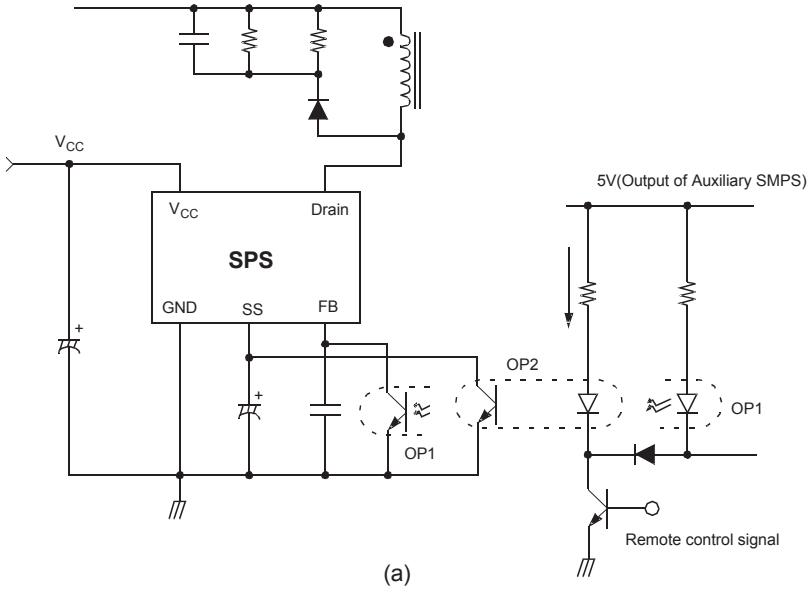
First, even if OP2 was eliminated and OP1 in the feedback terminal saturated, V_{CO} drops below 0.2V as mentioned before and the main power supply terminal stops switching and its operation stops. However, V_{SS} remains at 5V because the diode connected to the soft start terminal has been cut-off and, therefore, it cannot execute SPS soft start when the main power terminal is restarted. Therefore, to make the initial state or equal conditions to turn on/ off the main power supply terminal using the remote control, the soft start terminal must be “downed” to the GND level.

Furthermore, even when the soft start terminal OP2 is “downed” to the GND level and the feedback terminal OP1 left as is, V_{CO} drops below 0.2V and the main power supply terminal stops operating. However, the problem that arises at this point is that Vfb gradually increases due to the 5μA current supply source connected to the feedback terminal. When the feedback voltage reaches 7.5V, SPS latches -up due to the internal protection circuit and, once latched-up, the latched-up state does not release until V_{CC} falls below 5V. Therefore, even if the main power supply terminal is turned on by the remote control, the SPS remains latched-up and does not operate.

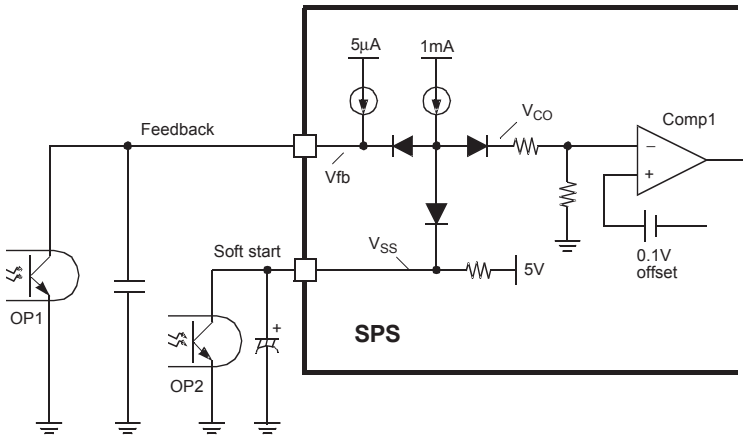
The feedback terminal potential is dropped to the GND level to prevent the feedback voltage from rising to 7.5V by flowing 5μA through OP1.

Though the method of cutting off the SPS V_{CC} power of the main power supply exists for remote control of the main power supply besides the above method, dropping the soft-start and feedback terminal voltages to GND level is simpler and effective in terms of circuitry for faster control based on the remote control signal. Figure 14 shows the application circuit of the PC SMPS, which require the auxiliary power supply, with SPS, above examined slope compensation and possible remote-On/ Off control.

The auxiliary power supply terminal has the flyback configuration primary regulation method with KA1H0165R and the main power supply terminal is designed to have the forward configuration with KA1M0880 allowing 5V and 12V outputs. The auxiliary power supply V_{CC} winding supplies the DC input to the SPS V_{CC} of the main power supply and, once the AC input power is supplied, the auxiliary power supply always operate normally.



(a)



(b)

Figure 13. Application circuit for remote control(a) and SPS internal block diagram(b)

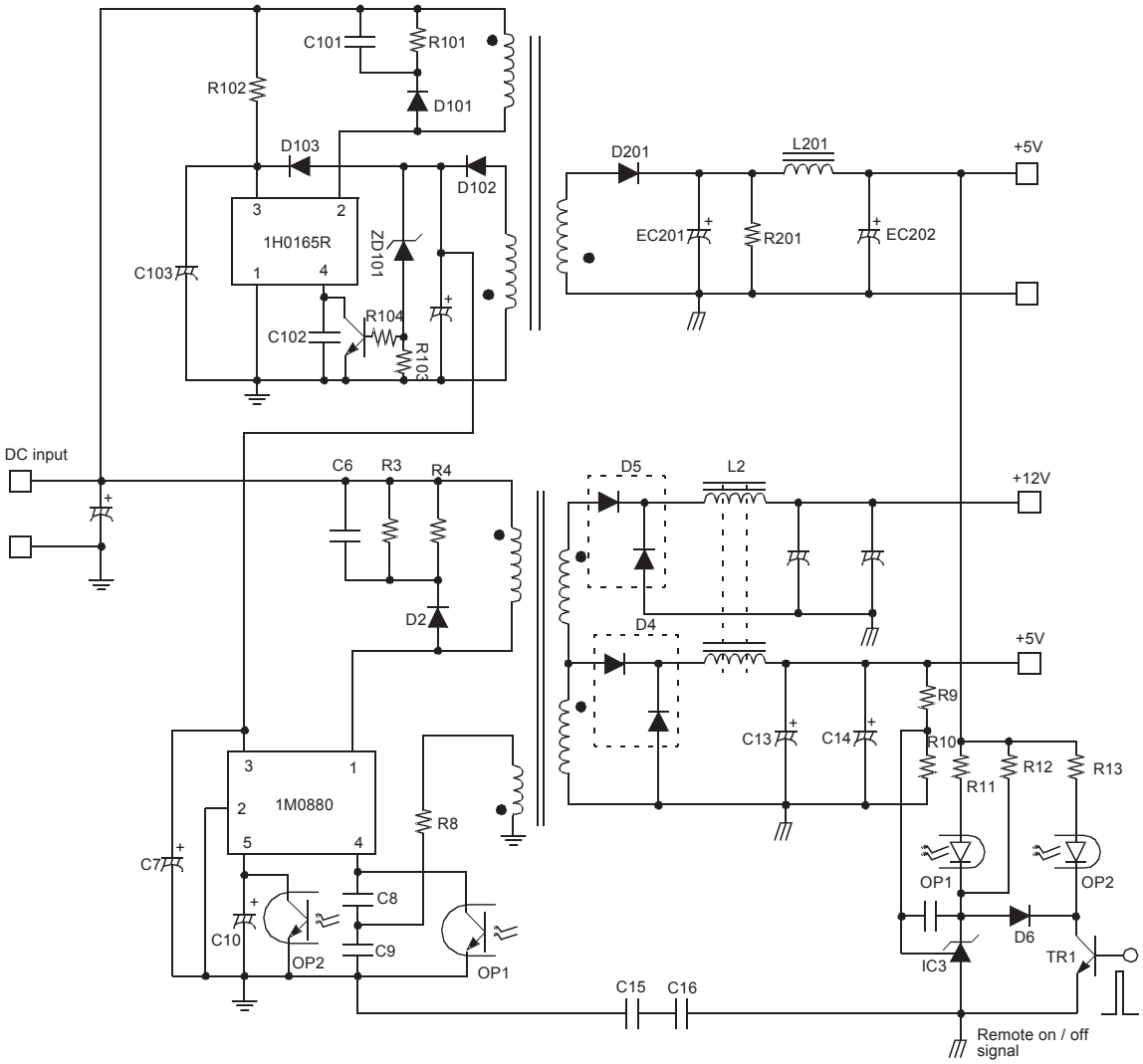


Figure 14. PC SMPS application circuit diagram with SPS and auxiliary power supply terminal remote on/off function

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3. KNOWN CAUTIONARY ITEMS WHEN DESIGNING TO APPLY THE SPS

Until now, the forward converter operation with SPS and SPS application circuit configuration method according to the various, special conditions of the PC SMPS were examined. Next, the known cautionary items when designing a circuit with SPS will be reviewed.

3.1 PCB Layout

Unlike the previous circuit which separated the switching element and the PWM control IC, the SPS combines the switching element (MOSFET) and the PWM IC into one package so the following items must be carefully considered when laying out the PCB.

One of the main items for caution when laying out the SMPS PCB is always the separation of the power GND and the Signal GND. The SPS package internally has a common GND so the power GND and Signal GND must be separated at the shortest possible point from the lead frame GND-Pin and the GND pattern length made shortest possible when laying out the PCB. (Refer to figure 15)

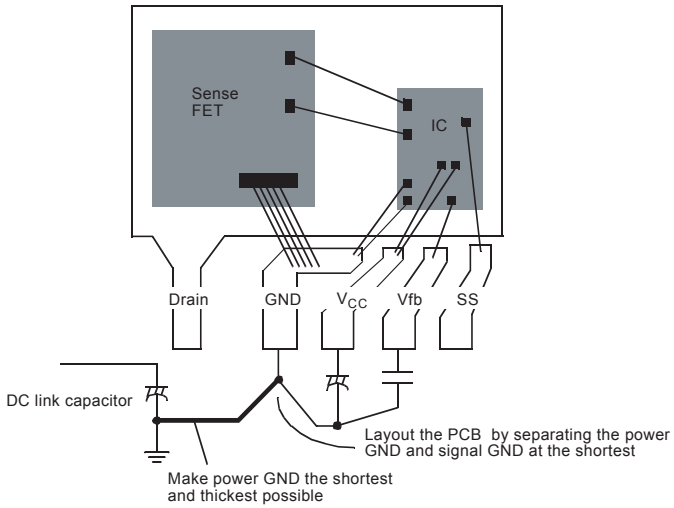

Figure 15. SPS lead frame and layout technique

3.2 Auxiliary Power Supply Switching Oscillation

The SPS PWM control is the Current Mode method. Though there are many advantages to the Current Mode Control, switching oscillation can be generated due to the noise in the sensing current if the output load decreases.

(Refer to Figure 16) The sensing current noise can greatly affect the PCB pattern, but, by using slope compensation as shown in Figure 16, the PCB could be designed more prudently. The standard values of the components used for slope compensation are presented in Figure 16. The above values is applicable to all flyback configured SMPS.

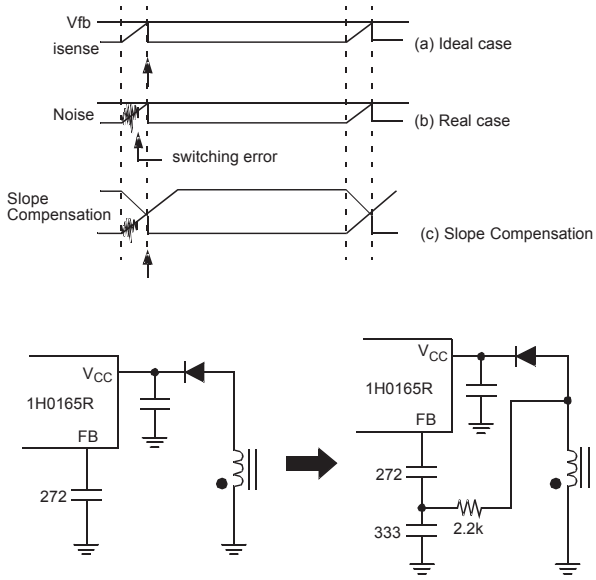

Figure 16. Origin for switching oscillation at no load and slope compensation application

Referance

[1] Switch Mode Power Supply Handbook, Keith H. Billings, McGraw-Hill, Inc., 1989

[2] “Coupled Filter Inductors in Multiple Output Buck Regulators Provide Dramatic Performance Improvement,” L. H. Dixon, Unitrode Seminar Manual SEM500

[3] “Modeling, Analysis and Compensation of the Current-Mode Converter”, Unitrode Application Note(U-97), Unitrode Linear Integrated Circuits Data Book and Applications Handbook

[4] Fairchild Semiconductor SPS Application Note, Fairchild Electronics, 1999

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