High Performance Multibit Σ-Δ DAC with SACD Playback

AD1955

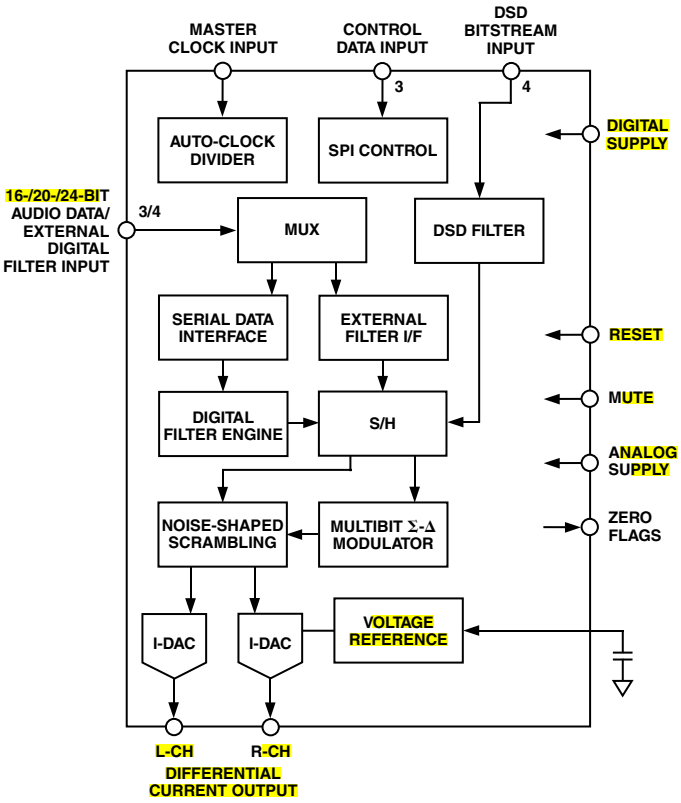
FEATURES

5 V Power Supply Stereo Audio DAC System
Accepts 16-/18-/20-/24-Bit Data
Supports 24-Bit, 192 kHz Sample Rate PCM Audio Data
Supports SACD Bit Stream and External Digital Filter Interface
Accepts a Wide Range of PCM Sample Rates Including: 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
Multibit Sigma-Delta Modulator with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
Data Directed Scrambling DAC—Low Sensitivity to Jitter
Supports SACD Playback with "Bit Expansion" Filter
Differential Current Output for Optimum Performance
8.64 mA p-p Differential Output
120 dB SNR/DNR (not muted) at 48 kHz Sample Rate (A-Weighted Stereo)
123 dB SNR/DNR (Mono)
–110 dB THD + N
110 dB Stop-Band Attenuation with ±0.0002 dB Pass-Band Ripple
8× Oversampling Digital Filter
On-Chip Clickless Volume Control
Supports SACD-Mute Pattern Detection
Supports 64 f_S/128 f_S DSD SACD with Phase Mode
Internal Digital Filter Pass-Through for External Filter
Master Clock: 256 f_S, 512 f_S, 768 f_S
Hardware and Software Controllable Clickless Mute
Serial (SPI) Control for Serial Mode, Number of Bits, Sample Rate, Volume, Mute, De-Emphasis, Mono Mode
Digital De-Emphasis for 32 kHz, 44.1 kHz, and 48 kHz Sample Rates
Flexible Serial Data Port with Right-Justified, Left-Justified, I^2S, and DSP Modes
28-Lead SSOP Plastic Package

APPLICATIONS

High End DVD Audio
SACD
CD
Home Theater Systems
Automotive Audio Systems
Sampling Musical Keyboards
Digital Mixing Consoles
Digital Audio Effects Processors

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The AD1955 is a complete, high performance, single-chip, stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, high performance digital interpolation filters, and continuous-time differential current output DACs. Other features include an on-chip clickless stereo attenuator and mute capability, programmed through an SPI compatible serial control port. The AD1955 is fully compatible with all known DVD audio formats including 192 kHz as well as 96 kHz sample frequencies and 24 bits. It is also backward compatible by supporting 50 µs/15 µs digital de-emphasis intended for "redbook" compact discs, as well as de-emphasis at 32 kHz and 48 kHz sample rates.

The AD1955 has a very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSPs, SACD decoders, external digital filters, AES/EBU receivers, and

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Serial Data Format in External Digital Filter Mode
In the External Digital Filter Mode, the AD1955 will accept up to 24-bit serial, twos complement, MSB-first data from an external digital filter, an HDCD decoder, or a general-purpose DSP. If the External Digital Filter Mode is selected by Control Register 0, Bits 12 and 13, Pin 2 to Pin 5 are assigned as the word clock input (EF_WCLK, Pin 2), bit clock input (EF_BCLK, Pin 3), left channel data input (EF_LDATA, Pin 4), and right channel data input (EF_RDATA, Pin 5), respectively, to accept $8f_S$ (48 kHz), $4f_S$ (96 kHz), or $2f_S$ (196 kHz) oversampled data.

Left and right channel data should be valid on the rising edge of EF_BCLK. The mode can be set to Left- or Right-Justified. A burst mode BCLK can be used in Left-Justified Mode.

Serial Data Format in SACD Mode
In the SACD Mode, the AD1955 supports both normal mode or phase modulation mode, which are selected by Control Register 1, Bit 6. If normal mode is selected, DSD_SCLK, DSD_LDATA, and DSD_RDATA are used to interface with DSD decoder chip. In this mode, the DSD data is clocked in the AD1955 using the rising edge of DSD_SCLK with a $64f_S$ rate, 2.8224 MHz. DSD_PHASE pin should be connected LOW.

If Phase Modulation Mode is selected, the DSD_PHASE pin is also used to interface with the DSD decoder. In this mode, a $64f_S$ DSD_PHASE signal is used as a reference signal to receive the data from the decoder. The DSD data is clocked into the AD1955 with a $128f_S$ DSD_SCLK.

The AD1955 can operate as a master or slave device. In Master Mode, the AD1955 will output DSD_SCLK and DSD_PHASE (if in Phase Modulation Mode) to a DSD decoder and will support Normal Mode and Phase Modulation Mode 0. In Slave Mode, the AD1955 will accept DSD_SCLK and DSD_PHASE (if in Phase Modulation Mode) from a DSD decoder and supports all of the normal and phase modulation modes.

When the SACD Port is not being used, the SACD pins (Pins 6, 7, 8, and 9) should be tied to a valid logic level. Please note that there are weak pull-ups (0.6 mA typical) on DSD_SCLK and DSD_PHASE.

Master Clock
The AD1955 must be set to the proper sample rate and master clock rate using Control Registers 0 and 1. The allowable master clock frequencies for each interpolation mode are shown below.

In the External Filter Mode, the AD1955 accepts master clock frequencies depending on the input sample rate as shown below.

In the SACD Mode, the AD1955 accepts a $256f_S$, $512f_S$, or $768f_S$ Master Clock, where f_S is nominally 44.1 kHz. In Slave Mode, by default, the rising edge of DSD_SCLK should coincide with the rising edge of MCLK. Control Register 1, Bit 2 should be set to 1 if the rising edge of DSD_SCLK coincides with the falling edge of MCLK. In Master Mode this bit can be used to select the MCLK edge used to generate the DSD clock outputs.

Zero Detection
When the AD1955 detects that the audio input data is continuously zero during 1024 LRCLK periods in PCM Mode or 8192 LRCLK periods in $8f_S$ External Digital Filter Mode, ZEROL (Pin 21) or ZEROR (Pin 20) is set to active.

When the AD1955 is in SACD Mode, it will detect an SACD mute pattern. If the input bit stream shows a mute pattern for about 22 ms, the AD1955 will set ZEROL (Pin 21) or ZEROR (Pin 20) to active. The outputs can be set to active high or low using Control Register 1, Bit 8.

Reset/Power-Down
The AD1955 will be reset when the $\overline{\text{PD/RST}}$ pin is set low. The part may be powered down using Bit 15, Control Register 0.

Audio Outputs
Active I/V converters should be used, which will hold the DAC outputs at a constant voltage level. Passive I/V conversion should not be used, since the DAC performance will be seriously degraded. For best THD + N performance over temperature, a reference voltage of 2.80 V should be used with the I/V converters. For a lower parts count, the voltage at FILTR can be used. In this instance, THD + N performance at high temperature can be improved by reducing I_{REF}, with an attendant reduction in gain (linear dependence) and DNR/SNR (square-root dependence).

The AD1955 audio outputs sink a current proportional to the input signal, superimposed on a steady bias current. The current-to-voltage (I/V) converters used need to be able to supply this bias current, as well as the signal current, or a resistor or current source can be used to a positive voltage to null this current in order to center the range of the I/V converters.

If pull-up resistors are used to bring the output of the I/V converters to 0 V for maximum headroom and THD balance, as shown in the applications circuits, the following equation can be used:

$$R_{PULLUP} = \left[V_{SUPPLY} - V_{BIAS}\right] / \left[I_{BIAS} + (V_{BIAS} / R_{I/V})\right]$$

PCM Mode

Interpolation Mode	Allowable Master Clock Frequencies (× f_S)								Nominal Input Sample Rate (kHz)
	64	96	128	192	256	384	512	768	
48 kHz (INT 8×) Mode					•		•	•	32, 44.1, 48
96 kHz (INT 4×) Mode			•		•	•			88.2, 96
192 kHz (INT 2×) Mode	•		•	•					176.4, 192

External Filter Mode

Input Sample Rate	Allowable Master Clock Frequencies (× f_S)								Nominal Input Sample Rate (to External Filter) (kHz)
	64	96	128	192	256	384	512	768	
8 × f_S					•		•	•	32, 44.1, 48
4 × f_S			•		•	•			88.2, 96
2 × f_S	•		•	•					176.4, 192

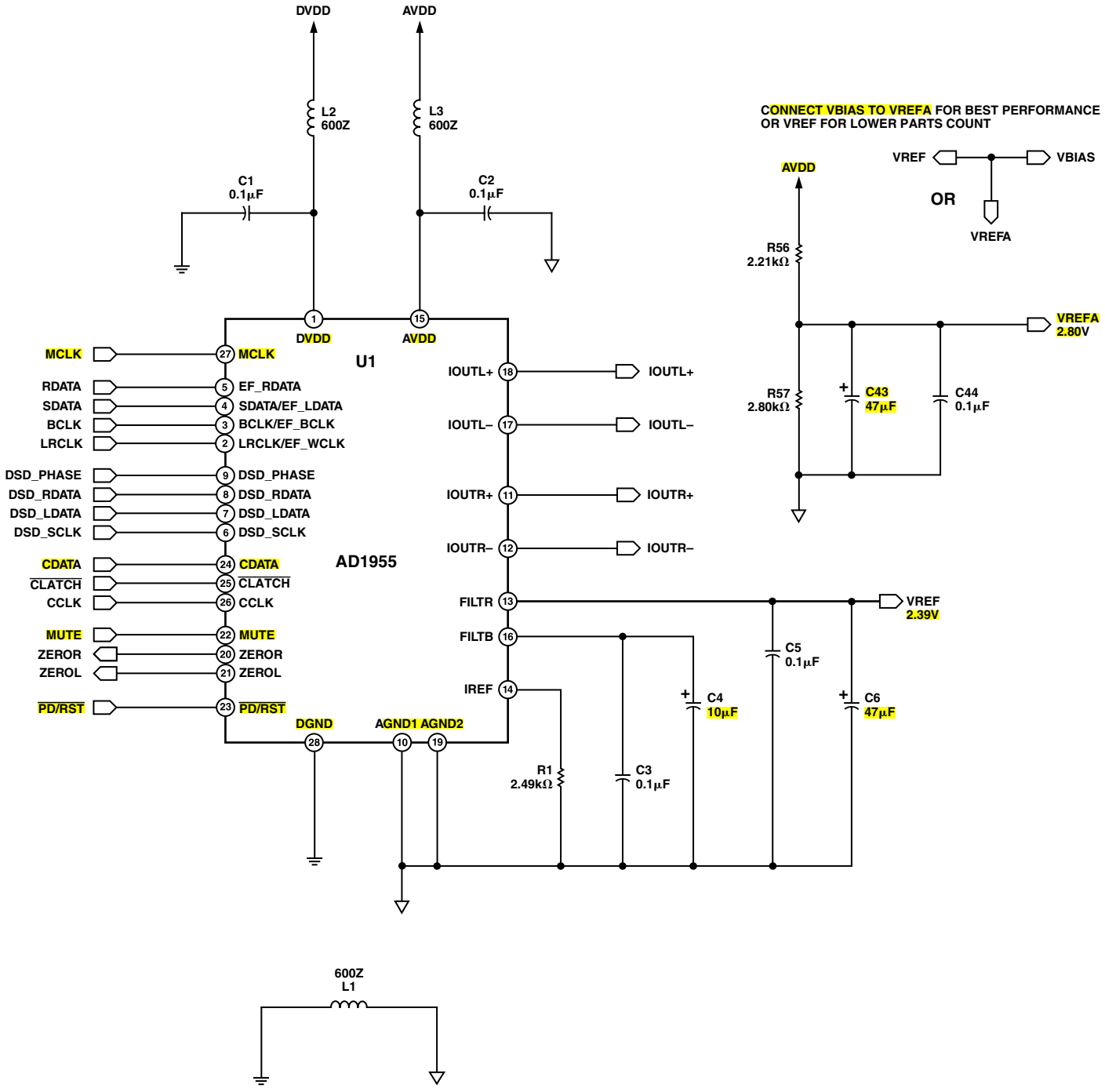

Figure 6. DAC Power Supply and Bypass

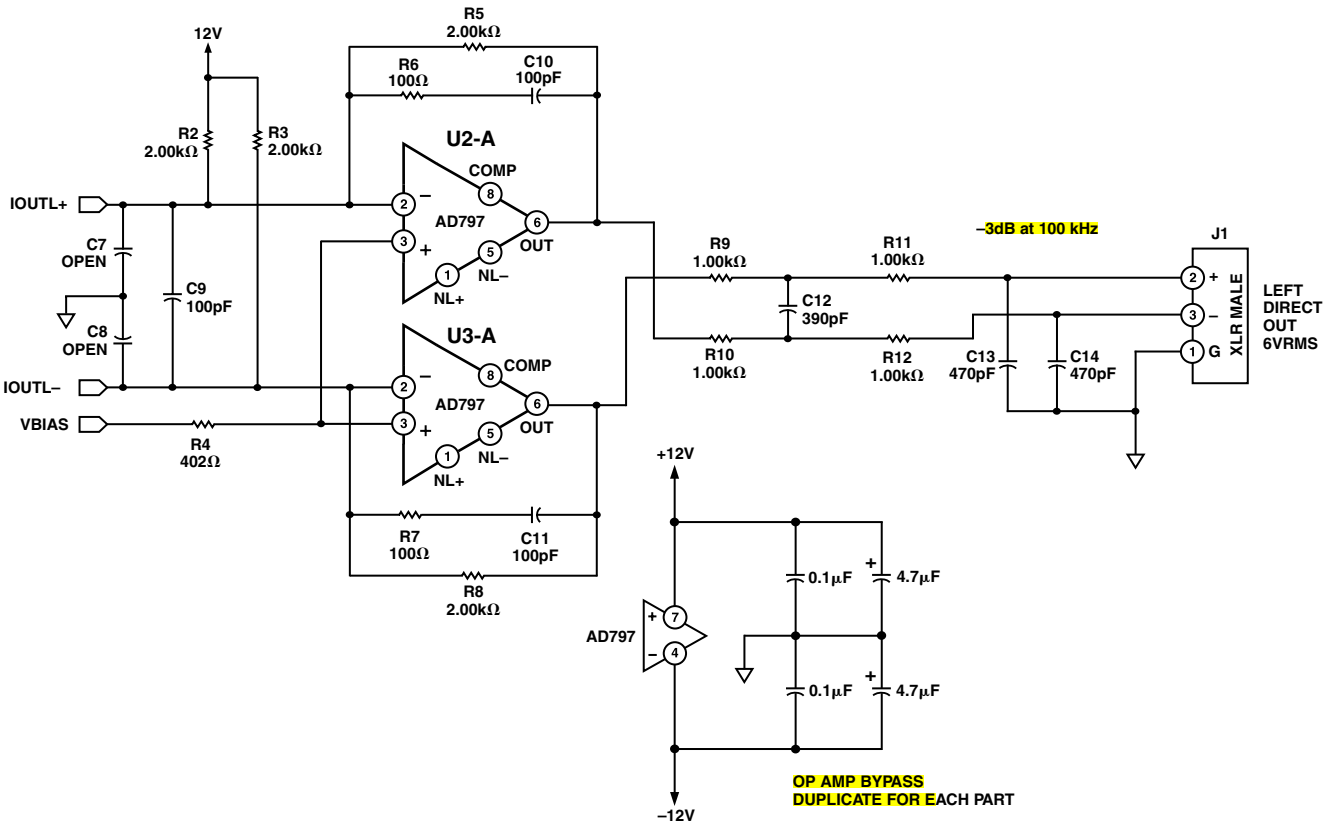

Figure 7. Left Channel Differential Output

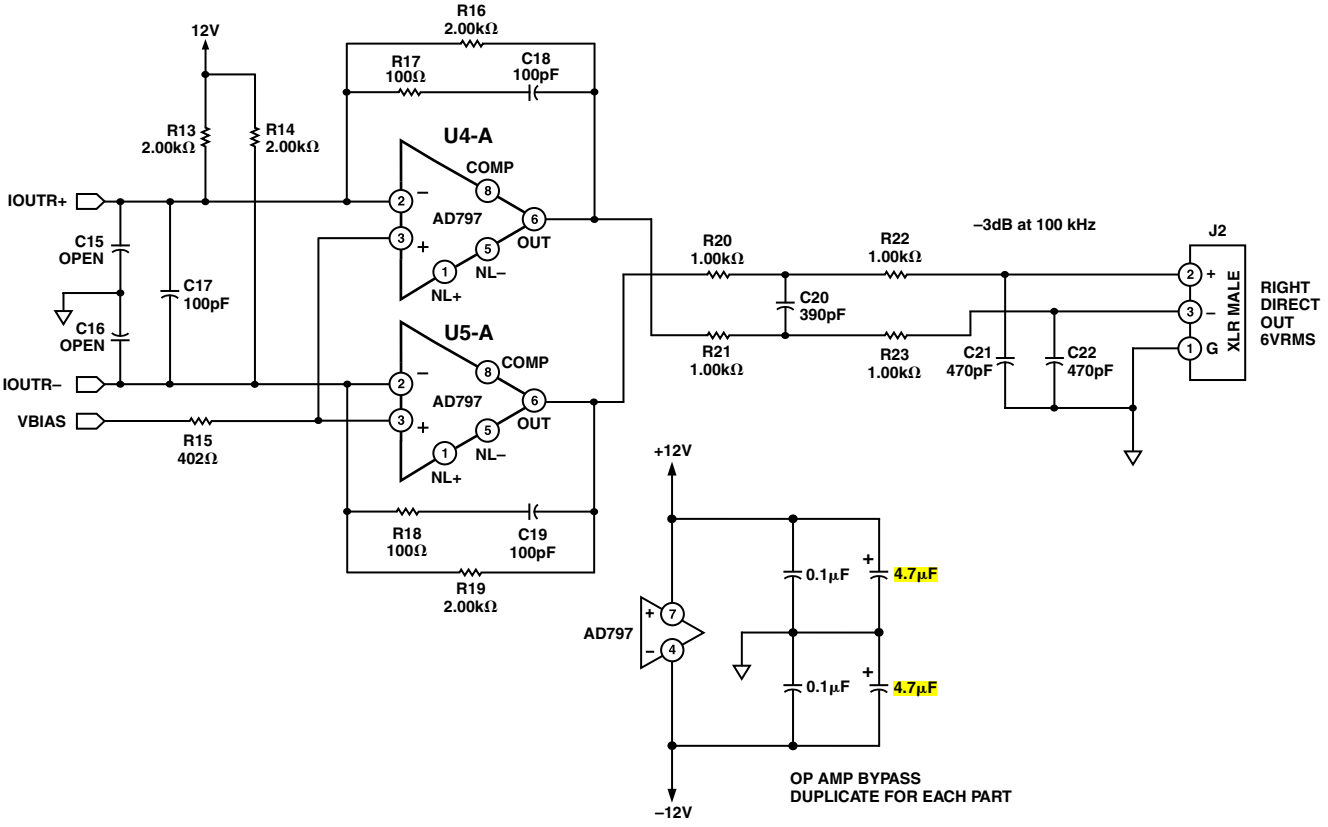

Figure 8. Right Channel Differential Output