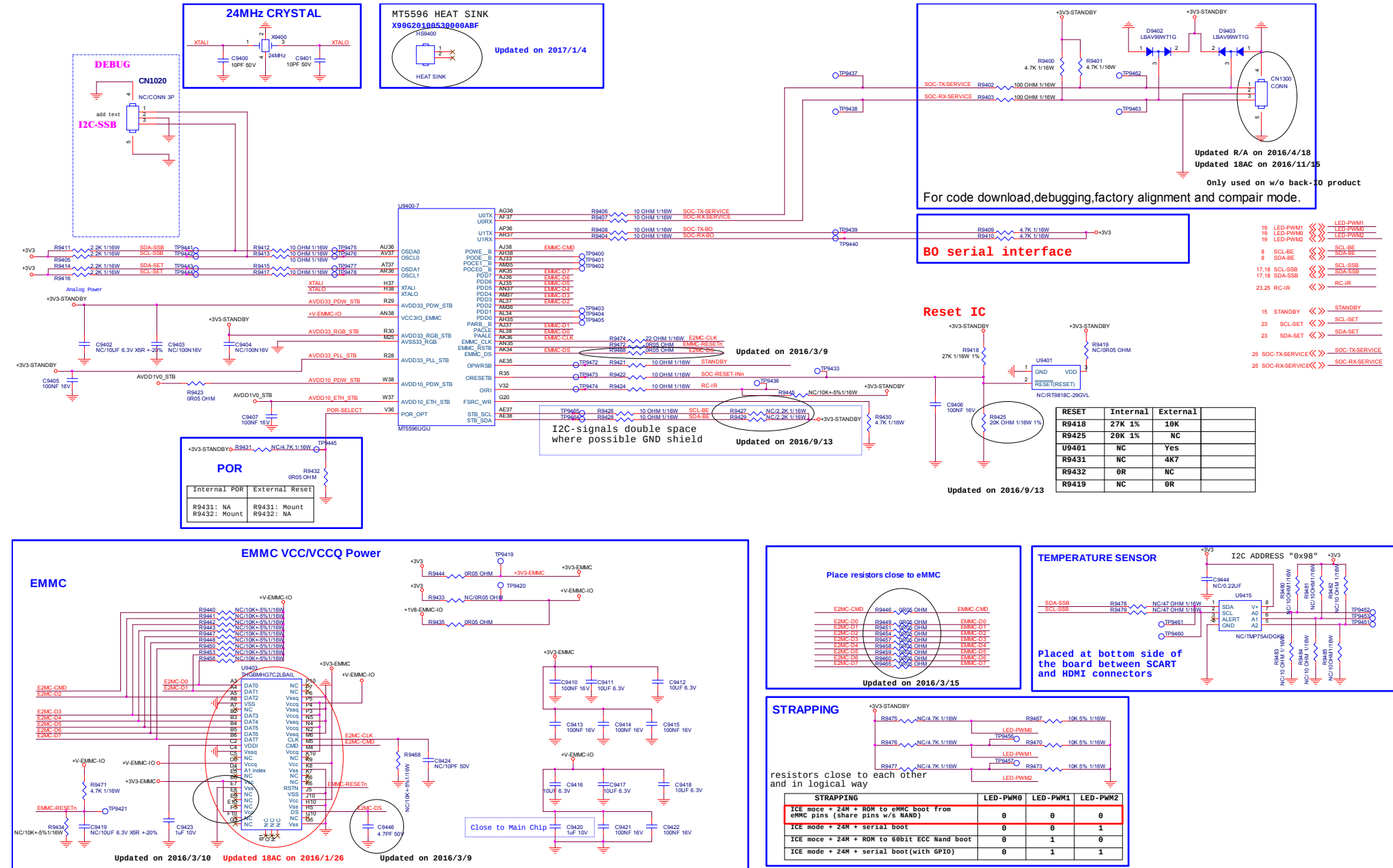
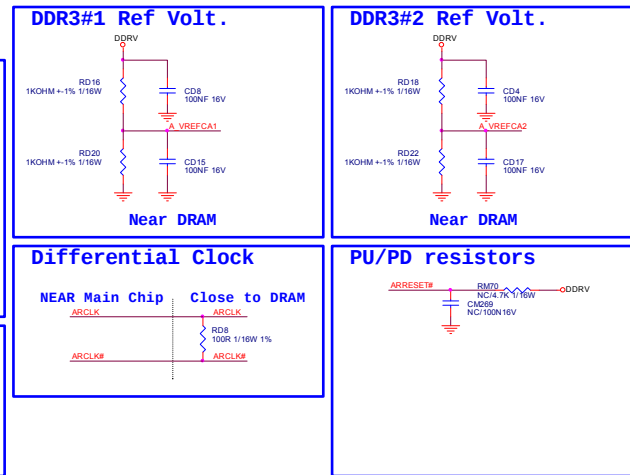
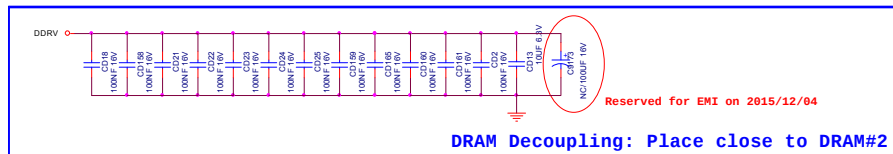
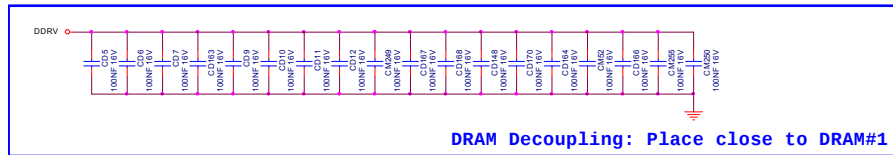
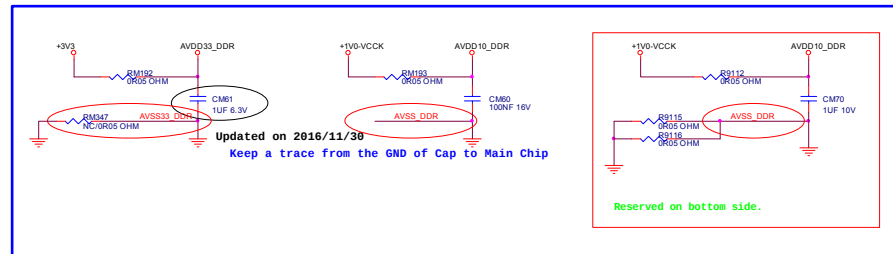
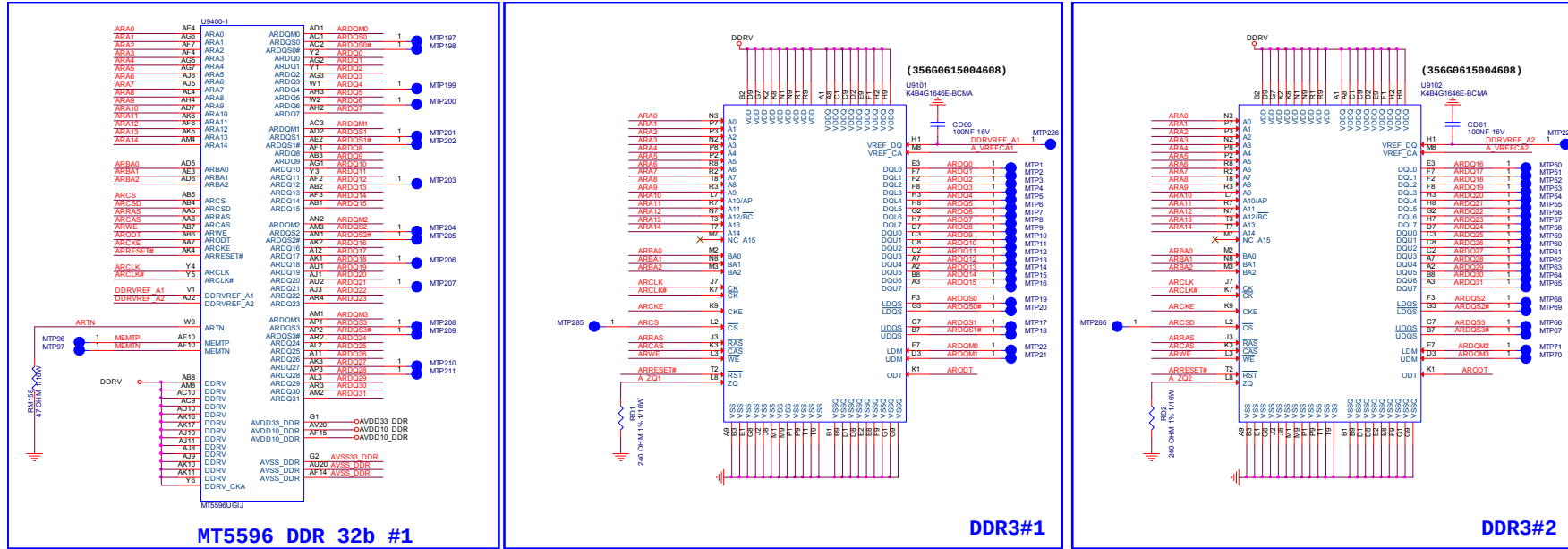


8-6-1 SOC-EMMC



8-6-2 SOC-DDR3-1-2



The image displays four detailed pinout diagrams for the MT5596 DDR 32b #2 memory module, showing connections for MT5596U, MT5596U, MT5596U, and MT5596U. Each diagram includes a table of pin numbers, signals, and functions, along with a physical pinout diagram showing the module's footprint and signal connections.

MT5596U Pinout Table:

Pin	Signal	Function
1	BRDQ0	1
2	BRDQ1	2
3	BRDQ2	3
4	BRDQ3	4
5	BRDQ4	5
6	BRDQ5	6
7	BRDQ6	7
8	BRDQ7	8
9	BRDQ8	9
10	BRDQ9	10
11	BRDQ10	11
12	BRDQ11	12
13	BRDQ12	13
14	BRDQ13	14
15	BRDQ14	15
16	BRDQ15	16
17	BRDQ16	17
18	BRDQ17	18
19	BRDQ18	19
20	BRDQ19	20
21	BRDQ20	21
22	BRDQ21	22
23	BRDQ22	23
24	BRDQ23	24
25	BRDQ24	25
26	BRDQ25	26
27	BRDQ26	27
28	BRDQ27	28
29	BRDQ28	29
30	BRDQ29	30
31	BRDQ30	31
32	BRDQ31	32

MT5596U Pinout Table:

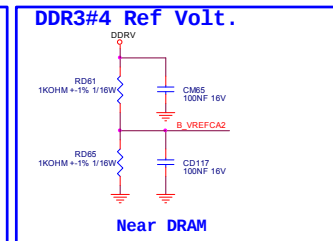
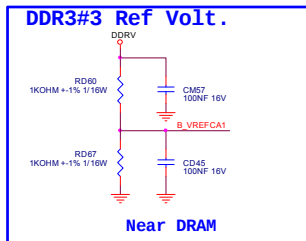
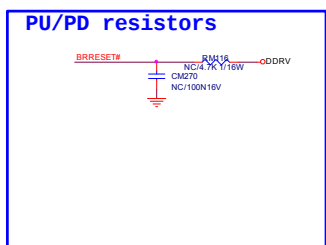
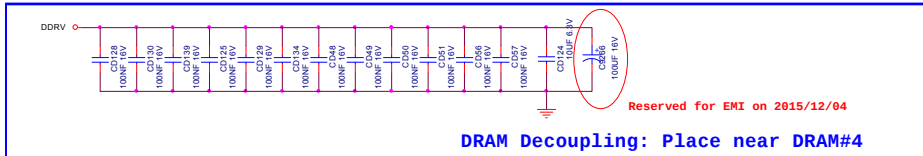
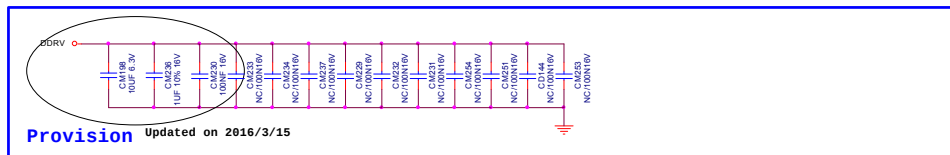
Pin	Signal	Function
1	BRDQ0	1
2	BRDQ1	2
3	BRDQ2	3
4	BRDQ3	4
5	BRDQ4	5
6	BRDQ5	6
7	BRDQ6	7
8	BRDQ7	8
9	BRDQ8	9
10	BRDQ9	10
11	BRDQ10	11
12	BRDQ11	12
13	BRDQ12	13
14	BRDQ13	14
15	BRDQ14	15
16	BRDQ15	16
17	BRDQ16	17
18	BRDQ17	18
19	BRDQ18	19
20	BRDQ19	20
21	BRDQ20	21
22	BRDQ21	22
23	BRDQ22	23
24	BRDQ23	24
25	BRDQ24	25
26	BRDQ25	26
27	BRDQ26	27
28	BRDQ27	28
29	BRDQ28	29
30	BRDQ29	30
31	BRDQ30	31
32	BRDQ31	32

MT5596U Pinout Table:

Pin	Signal	Function
1	BRDQ0	1
2	BRDQ1	2
3	BRDQ2	3
4	BRDQ3	4
5	BRDQ4	5
6	BRDQ5	6
7	BRDQ6	7
8	BRDQ7	8
9	BRDQ8	9
10	BRDQ9	10
11	BRDQ10	11
12	BRDQ11	12
13	BRDQ12	13
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32	BRDQ31	32

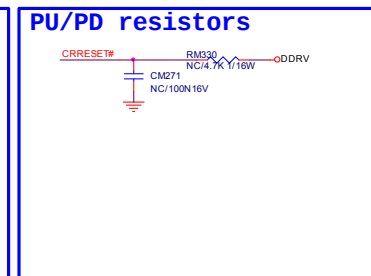
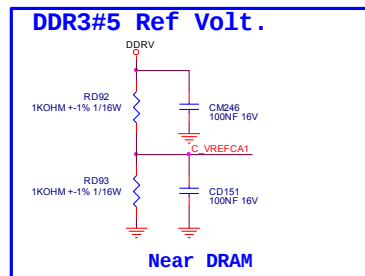
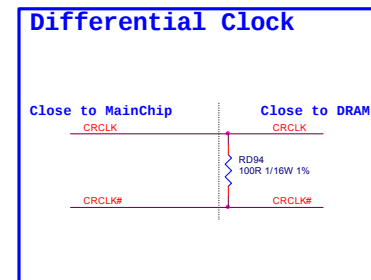
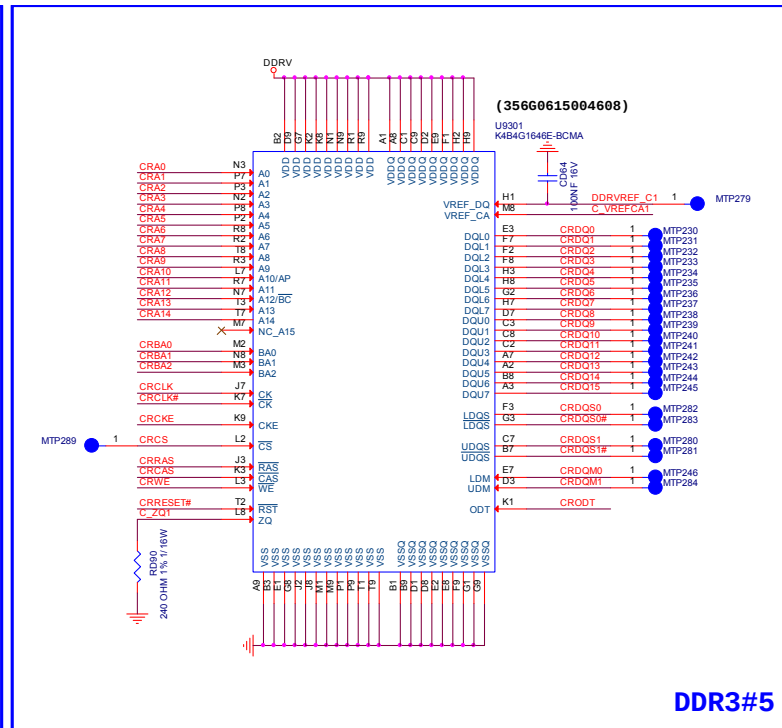
MT5596U Pinout Table:

Pin	Signal	Function
1	BRDQ0	1
2	BRDQ1	2
3	BRDQ2	3
4	BRDQ3	4
5	BRDQ4	5
6	BRDQ5	6
7	BRDQ6	7
8	BRDQ7	8
9	BRDQ8	9
10	BRDQ9	10
11	BRDQ10	11
12	BRDQ11	12
13	BRDQ12	13
14	BRDQ13	14
15	BRDQ14	15
16	BRDQ15	16
17	BRDQ16	17
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31	BRDQ30	31
32	BRDQ31	32

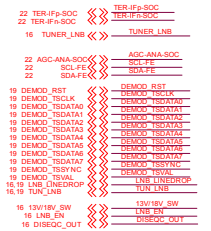
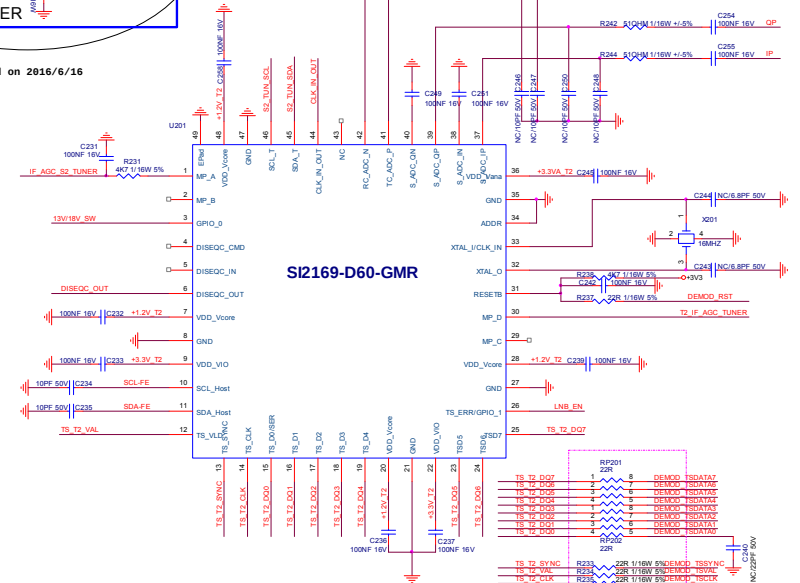
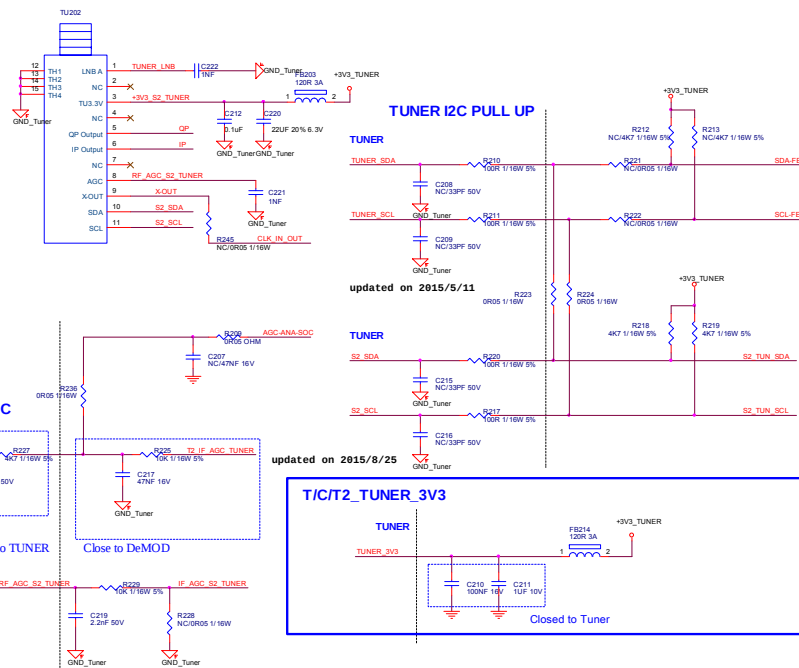
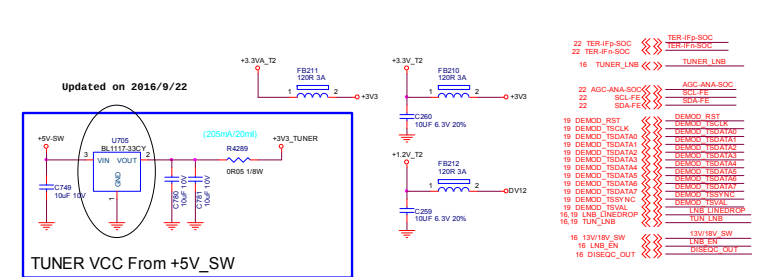
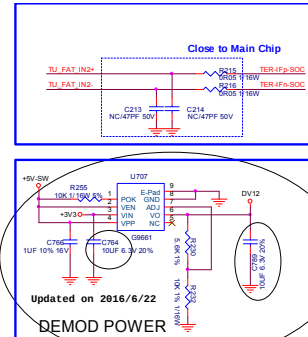
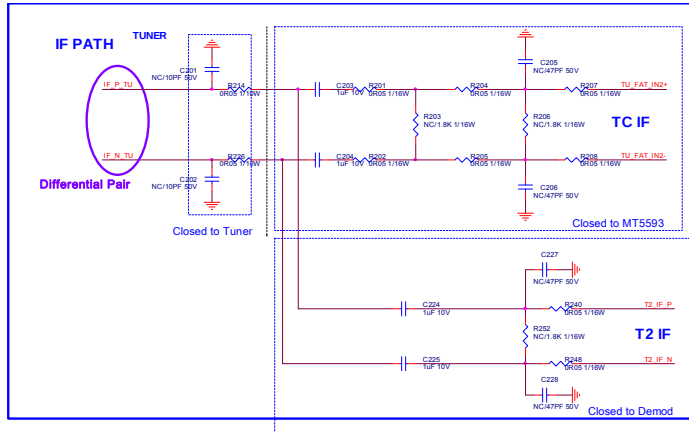
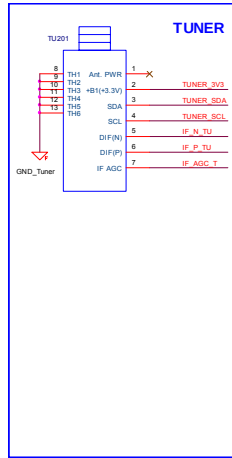


Pin-to-pin comparison diagram for MT5596 DDR 16b. The diagram shows two columns of pins and their corresponding functions. The left column lists pins from U9400-13 to U9400-13, and the right column lists pins from N1 to N12. The bottom section shows a circuit diagram for the DDR0_V0 pin, which is connected to a 47 OHM resistor and a 1.8V supply. The circuit also shows the connection of the DDR0_V0 pin to the DDR0_V0 pin of the MT5596U01U1 package.

Pin	Function	Pin	Function
CRA0	J5	CRDQM0	N1
CRA1	U2	CRDQ00	N3
CRA2	K7	CRDQ01	N2
CRA3	J4	CRDQ02	N2
CRA4	U4	CRDQ03	K2
CRA5	K8	CRDQ04	T2
CRA6	U9	CRDQ05	J2
CRA7	H7	CRDQ06	U2
CRA8	U8	CRDQ07	H2
CRA9	H8	CRDQ08	V2
CRA10	I8	CRDQ09	H3
CRA11	R6	CRDQ10	U1
CRA12	U4	CRDQ11	CRDQ1
CRA13	H5	CRDQ12	M3
CRA14	U7	CRDQ13	P2
		CRDQ14	P1
		CRDQ15	K3
		CRDQ16	K3
		CRDQ17	R2
		CRDQ18	K1
		CRDQ19	F3
		CRDQ20	L1
		CRDQ21	R1
		CRDQ22	L2
		CRDQ23	R2
		CRDQ24	K1
		CRDQ25	F3
		CRDQ26	L1
		CRDQ27	R1
		CRDQ28	L2
		CRDQ29	R2
		CRDQ30	K1
		CRDQ31	F3
		CRDQ32	L1
		CRDQ33	R1
		CRDQ34	L2
		CRDQ35	R2
		CRDQ36	K1
		CRDQ37	F3
		CRDQ38	L1
		CRDQ39	R1
		CRDQ40	L2
		CRDQ41	R2
		CRDQ42	K1
		CRDQ43	F3
		CRDQ44	L1
		CRDQ45	R1
		CRDQ46	L2
		CRDQ47	R2
		CRDQ48	K1
		CRDQ49	F3
		CRDQ50	L1
		CRDQ51	R1
		CRDQ52	L2
		CRDQ53	R2
		CRDQ54	K1
		CRDQ55	F3
		CRDQ56	L1
		CRDQ57	R1
		CRDQ58	L2
		CRDQ59	R2
		CRDQ60	K1
		CRDQ61	F3
		CRDQ62	L1
		CRDQ63	R1
		CRDQ64	L2
		CRDQ65	R2
		CRDQ66	K1
		CRDQ67	F3
		CRDQ68	L1
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		CRDQ70	L2
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		CRDQ77	R2
		CRDQ78	K1
		CRDQ79	F3
		CRDQ80	L1
		CRDQ81	R1
		CRDQ82	L2
		CRDQ83	R2
		CRDQ84	K1
		CRDQ85	F3
		CRDQ86	L1
		CRDQ87	R1
		CRDQ88	L2
		CRDQ89	R2
		CRDQ90	K1
		CRDQ91	F3
		CRDQ92	L1
		CRDQ93	R1
		CRDQ94	L2
		CRDQ95	R2
		CRDQ96	K1
		CRDQ97	F3
		CRDQ98	L1
		CRDQ99	R1
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8-6-5 FE-TUNER-DEMOD-TPV



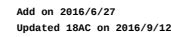
MT5596 Vx1 OUTPUT



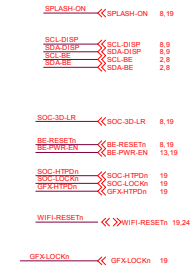
Updated on 2017/1/13
Updated on 2016/12/14



MT5596 Vx1 OUTPUT for Debug

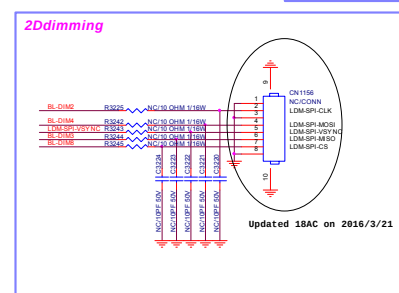
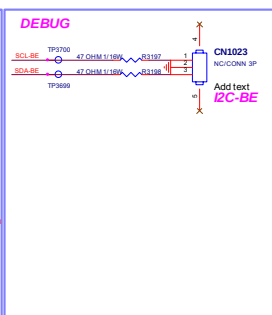
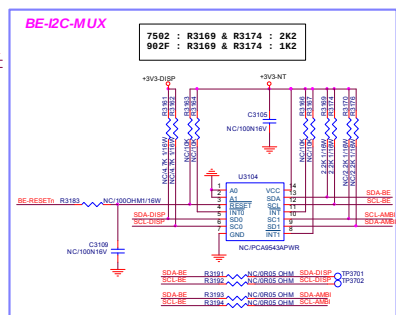
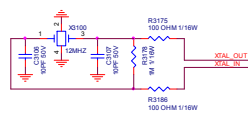
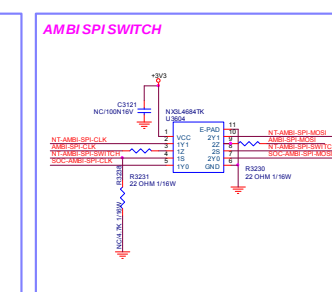
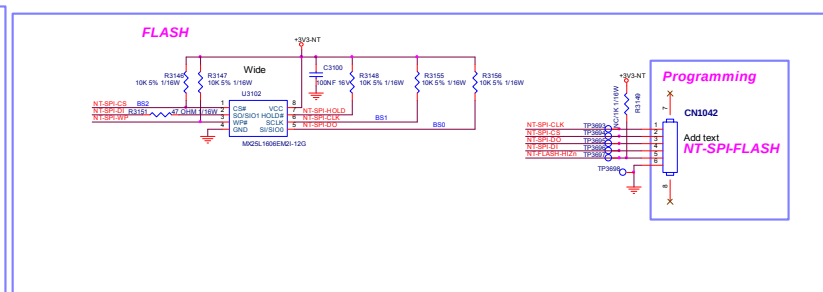
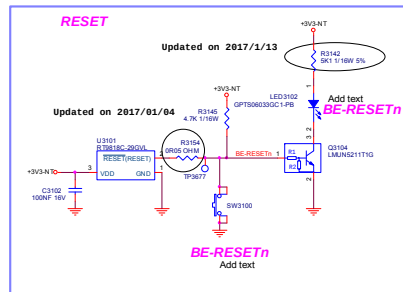
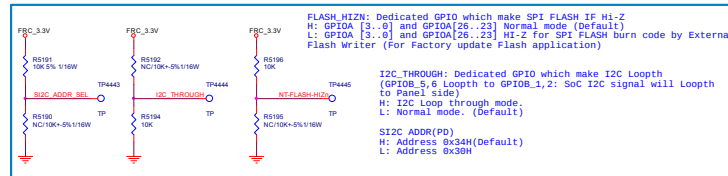
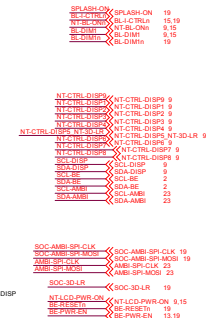
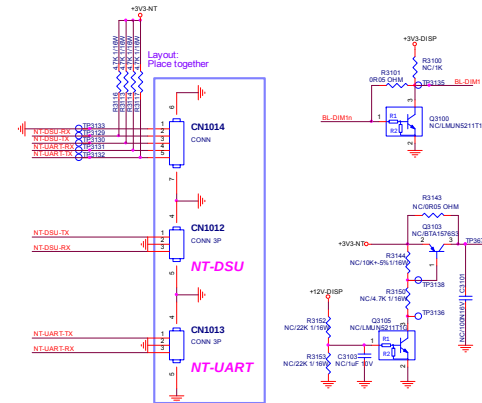
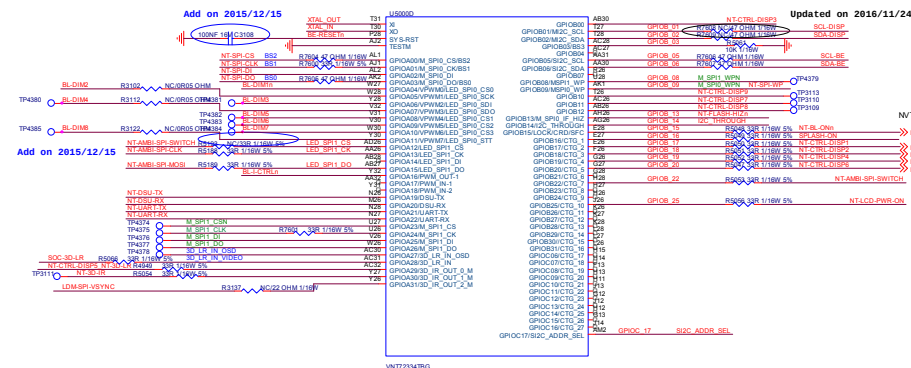


Add on 2015/10/23

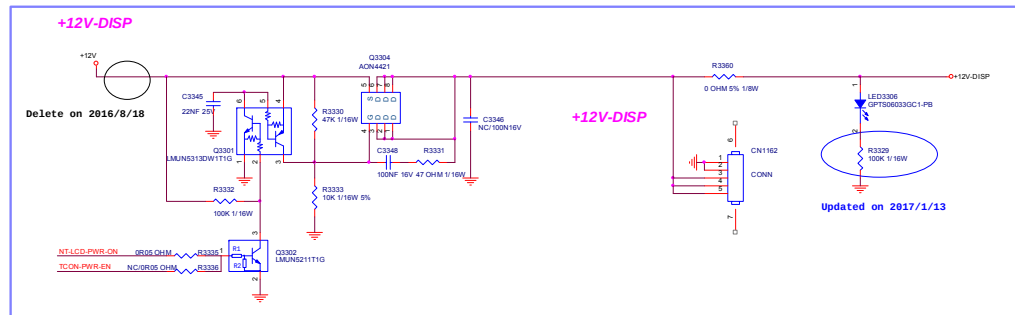
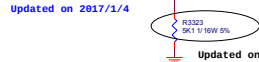


8-6-7 BE-NT7234b-GPIO

NT334 CONTROL



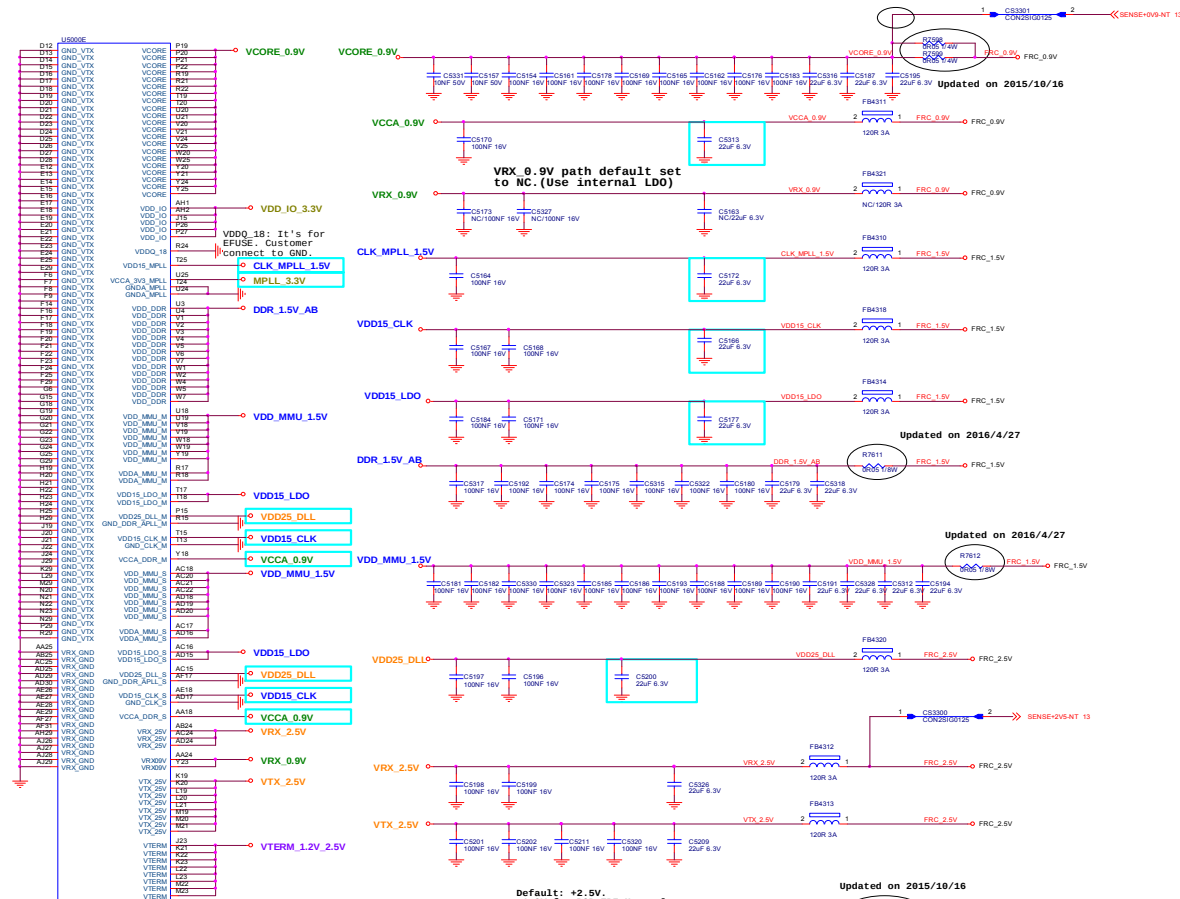
NT334 V-BY-1 OUTPUT



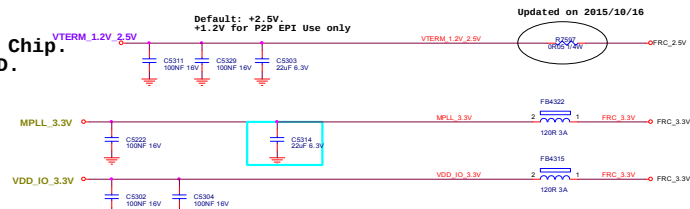
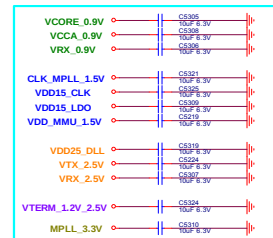
8-6-9 BE-NT7234d-POWER

NT334 POWER

Updated on 2015/10/28



RESERVE HEAT-SINK AREA for Main Chip.
Suggest HEAT-SINK Connect to GND.



The POWER CAP PLACE NEAR Main IC

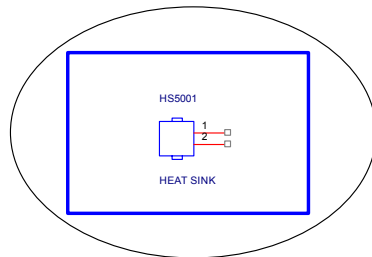
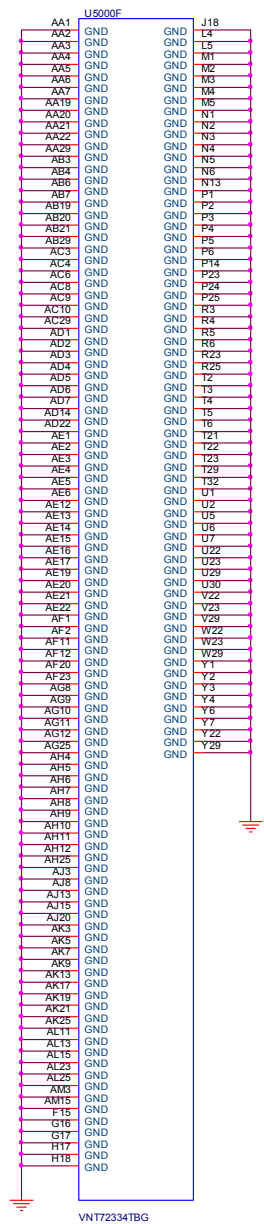
Please add a 22uF cap for the CLK/DLL/MPLL power IF.

These POWER CAP PLACE at Layer4, just for debug use.

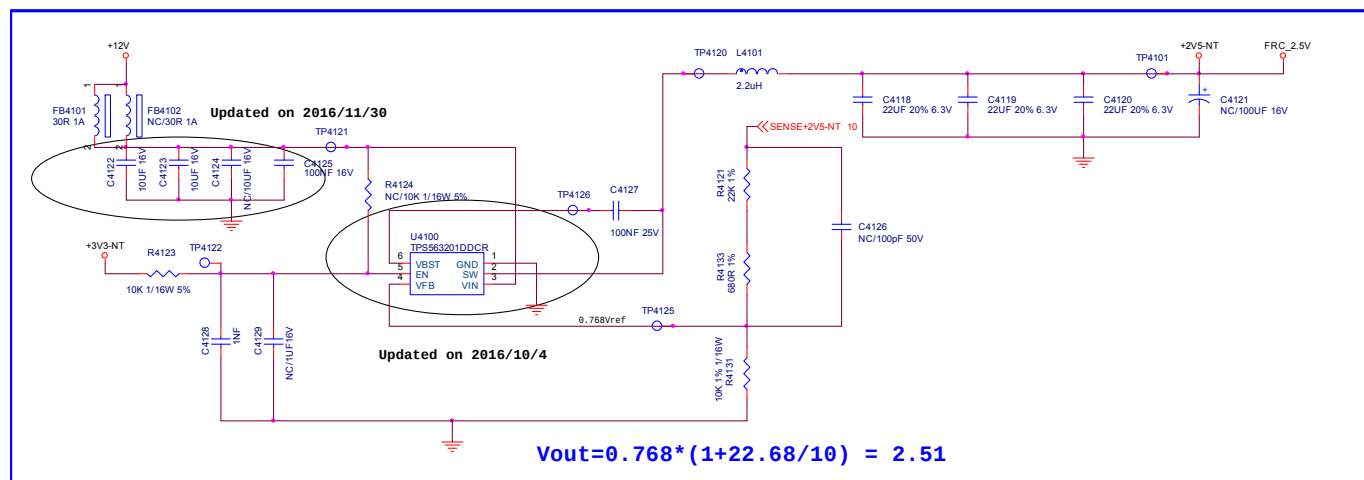
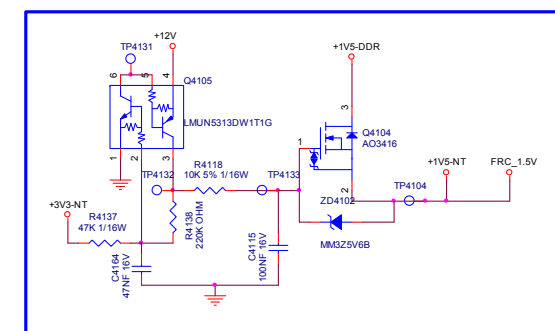
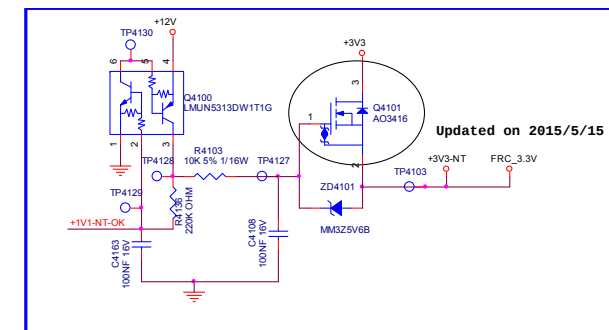
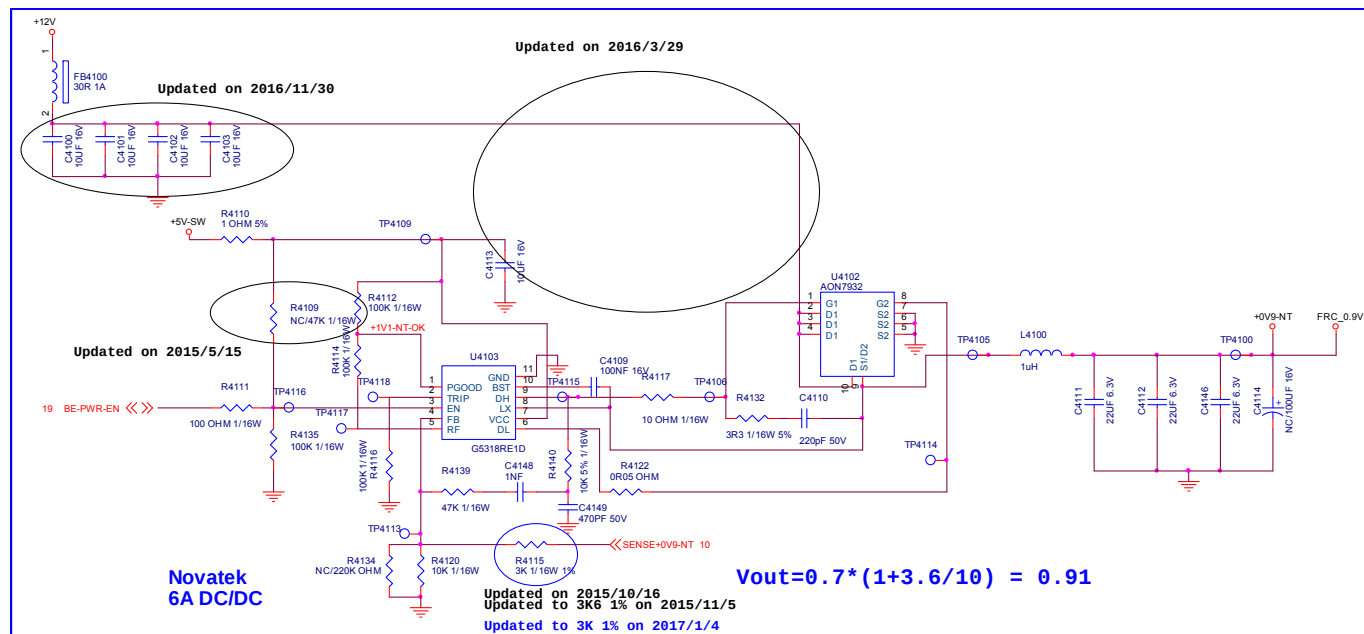
NT334 DDR A-B



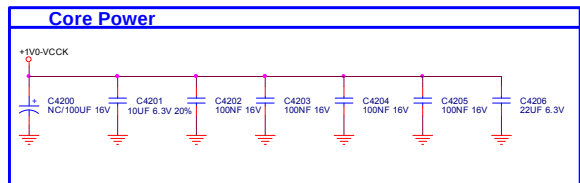
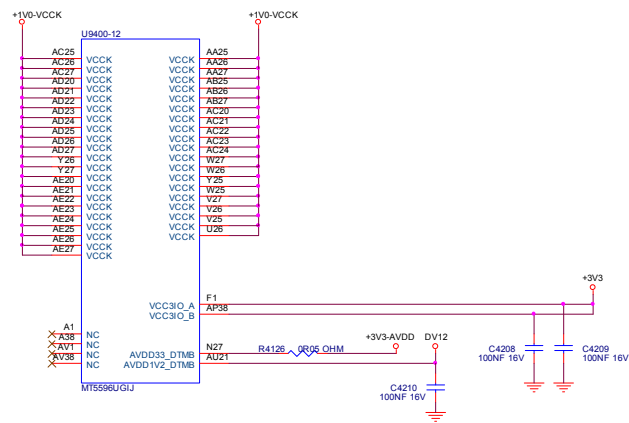
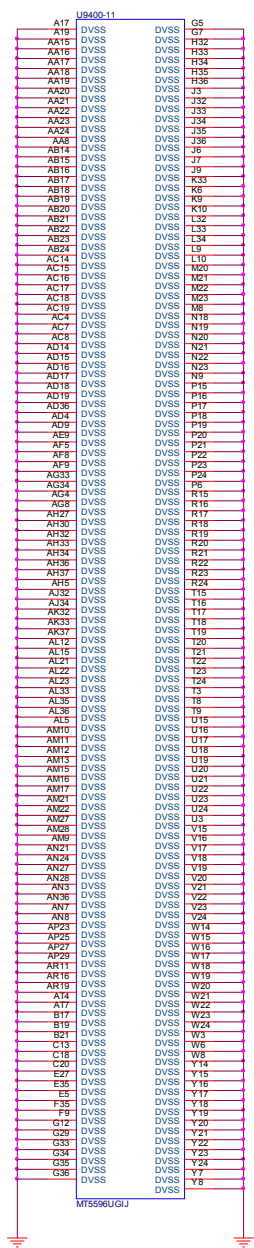
NT334 GROUND



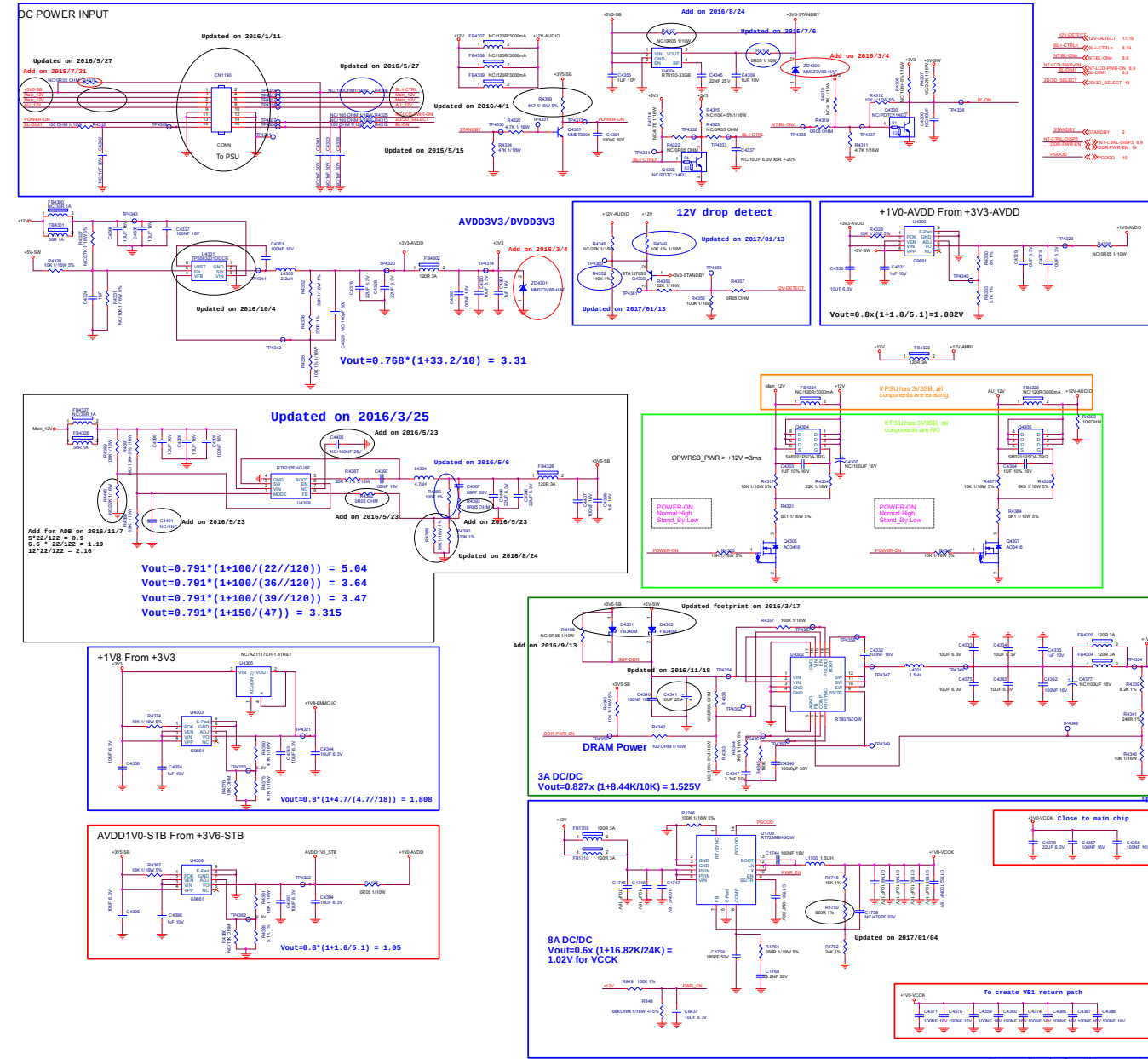
8-6-12 DCDC-Novatek-POWER

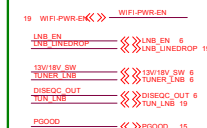
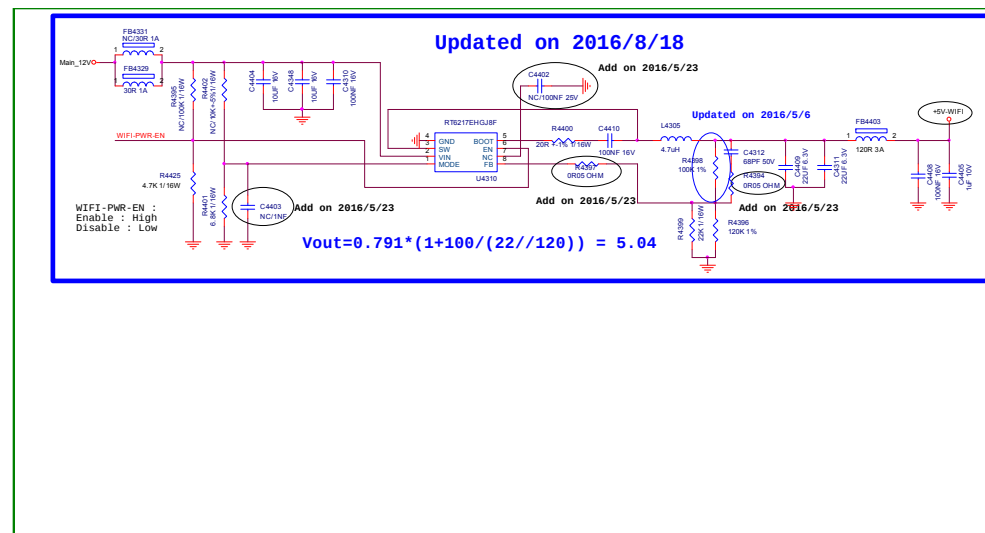


8-6-13 DCDC-SOC-VCCK-DVSS

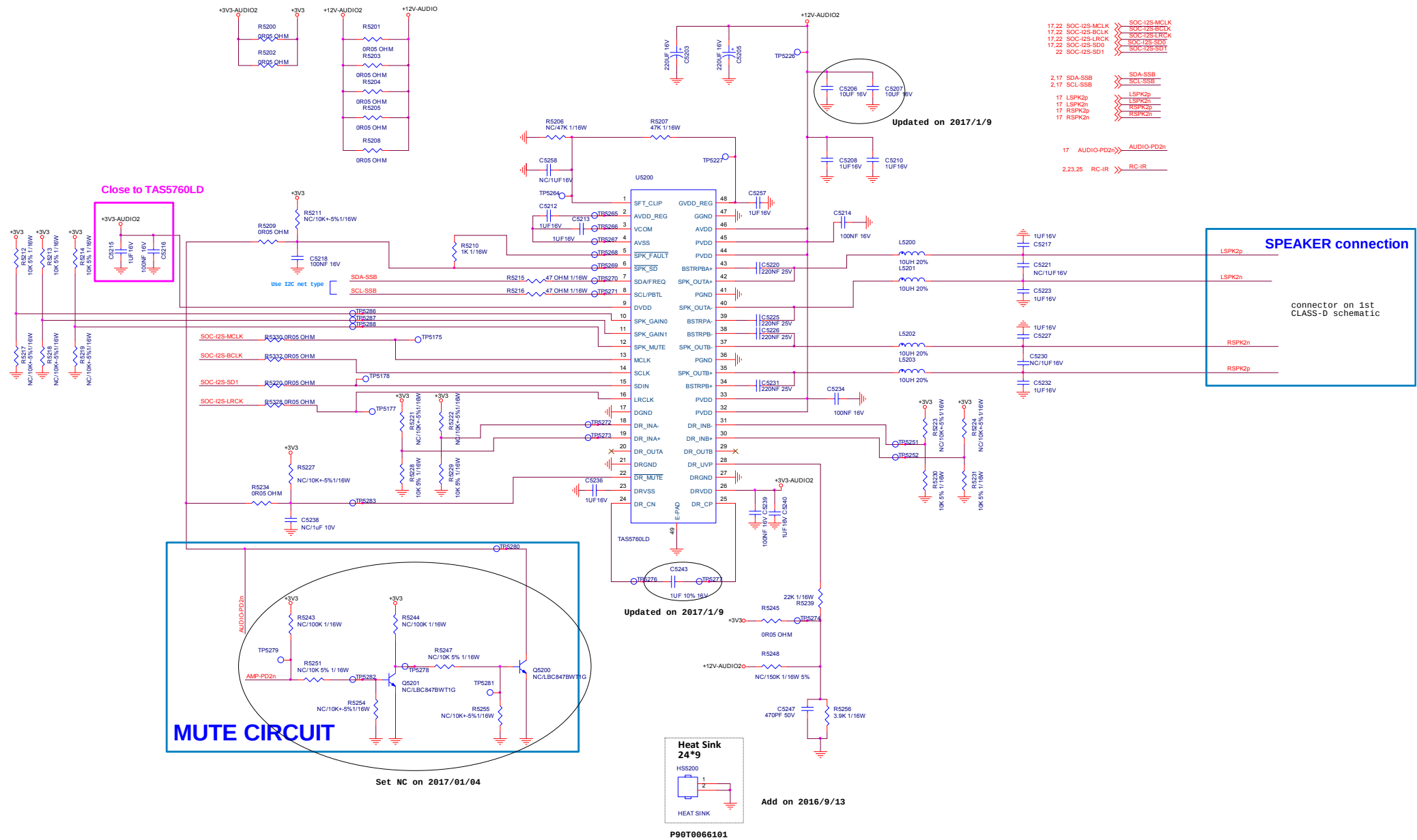


8-6-14 DCDC-SYSTEM-POWER1

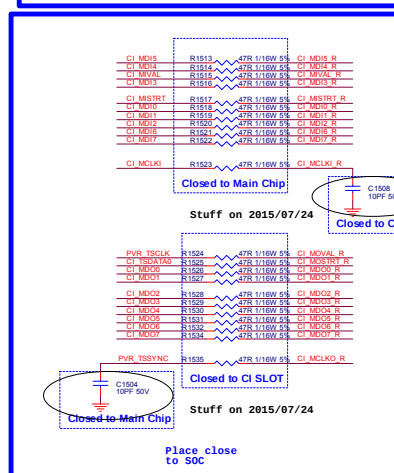
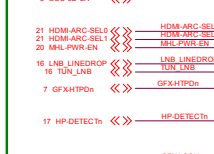
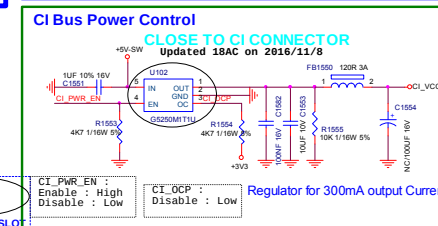
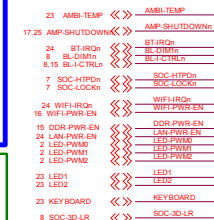
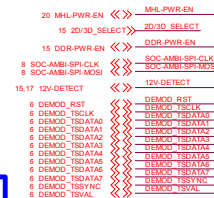
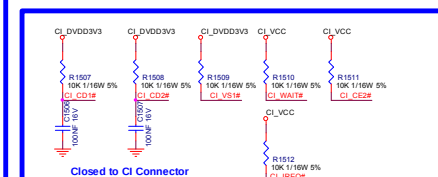
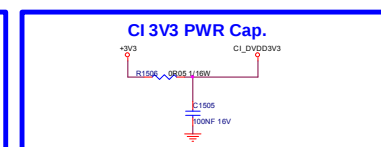
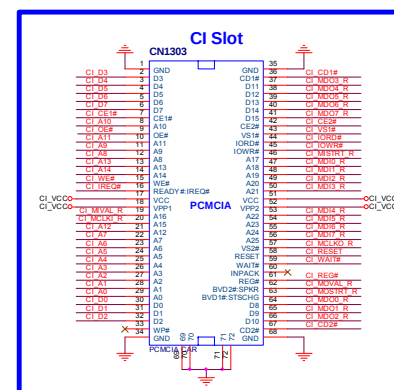
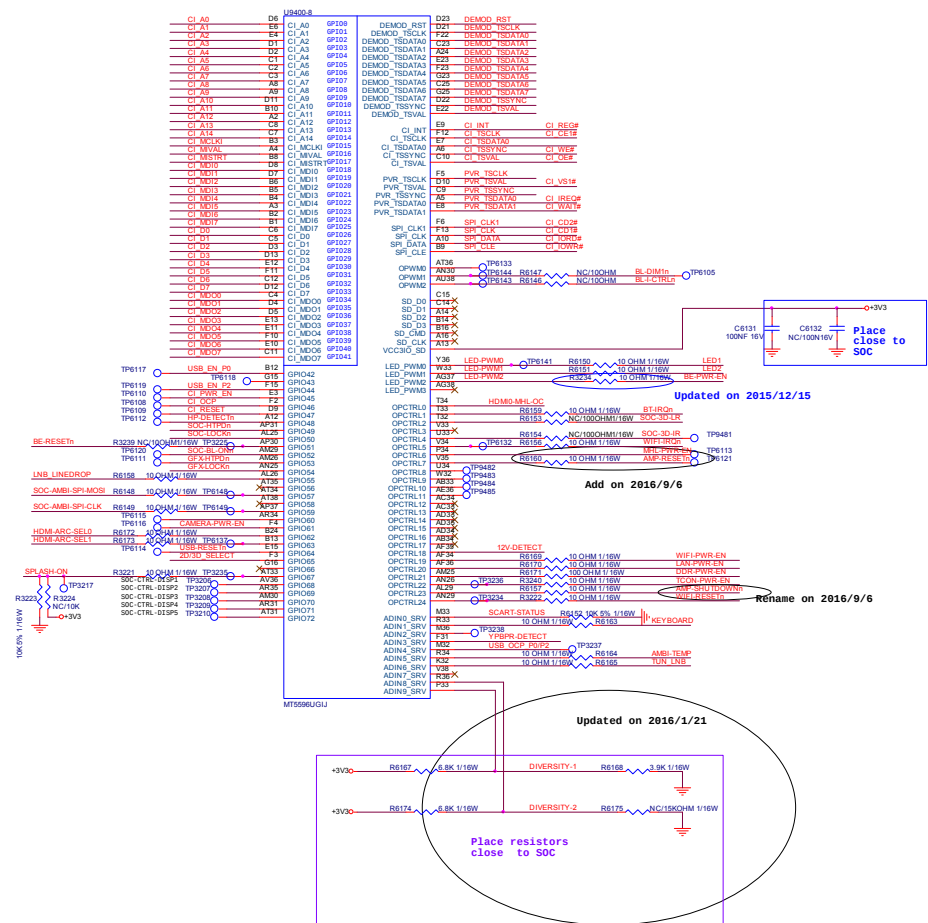


[illegible][illegible][illegible]

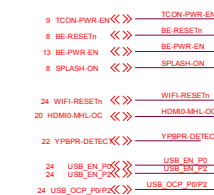
8-6-18 AUDIO-2nd-CLASS-D-AMP



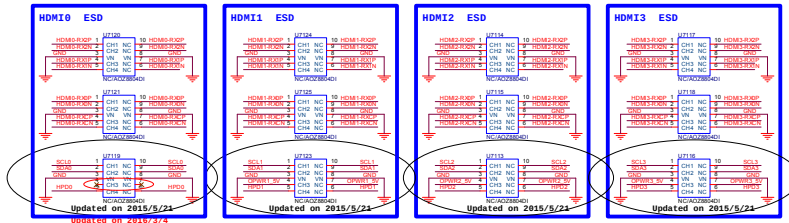
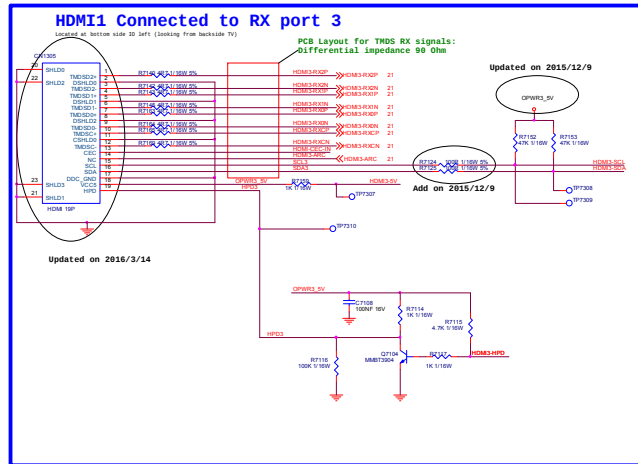
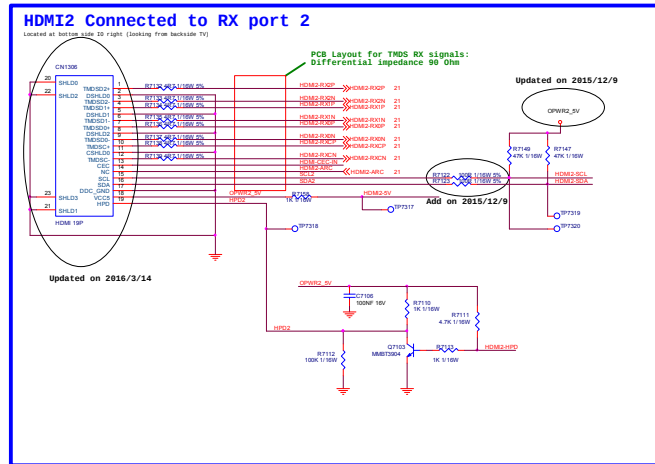
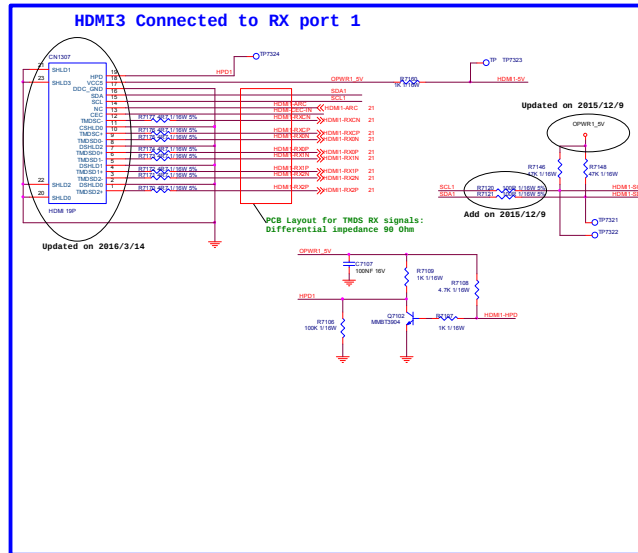
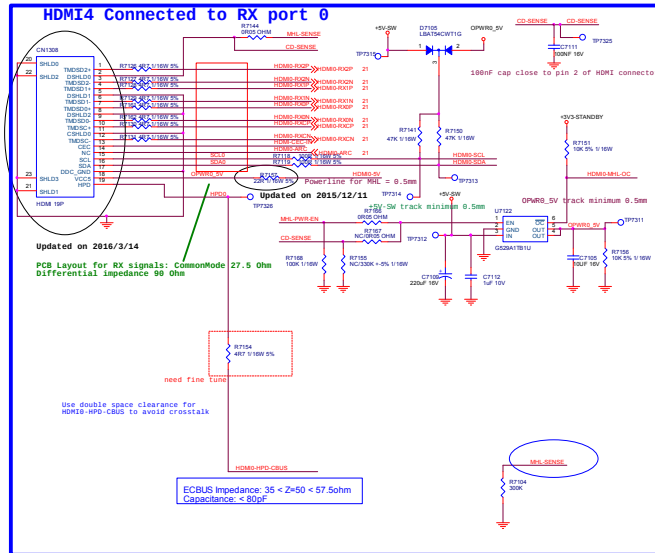
8-6-19 PCMCIA



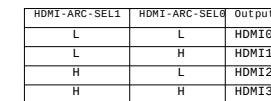
Parrel TS Output to PCMCIA damping used to close Main Chip	Parrel TS Output to Main Chip damping used to close PCMCIA
CI_MISTR1	CI_MISTR1
CI_MIVAL	CI_MIVAL
CI_MCLKI	CI_MCLK0
CI_MDI0	CI_MDI00
CI_MDI1	CI_MDI01
CI_MDI2	CI_MDI02
CI_MDI3	CI_MDI03
CI_MDI4	CI_MDI04
CI_MDI5	CI_MDI05
CI_MDI6	CI_MDI06
CI_MDI7	CI_MDI07



8-6-20 HDMI-INPUTS

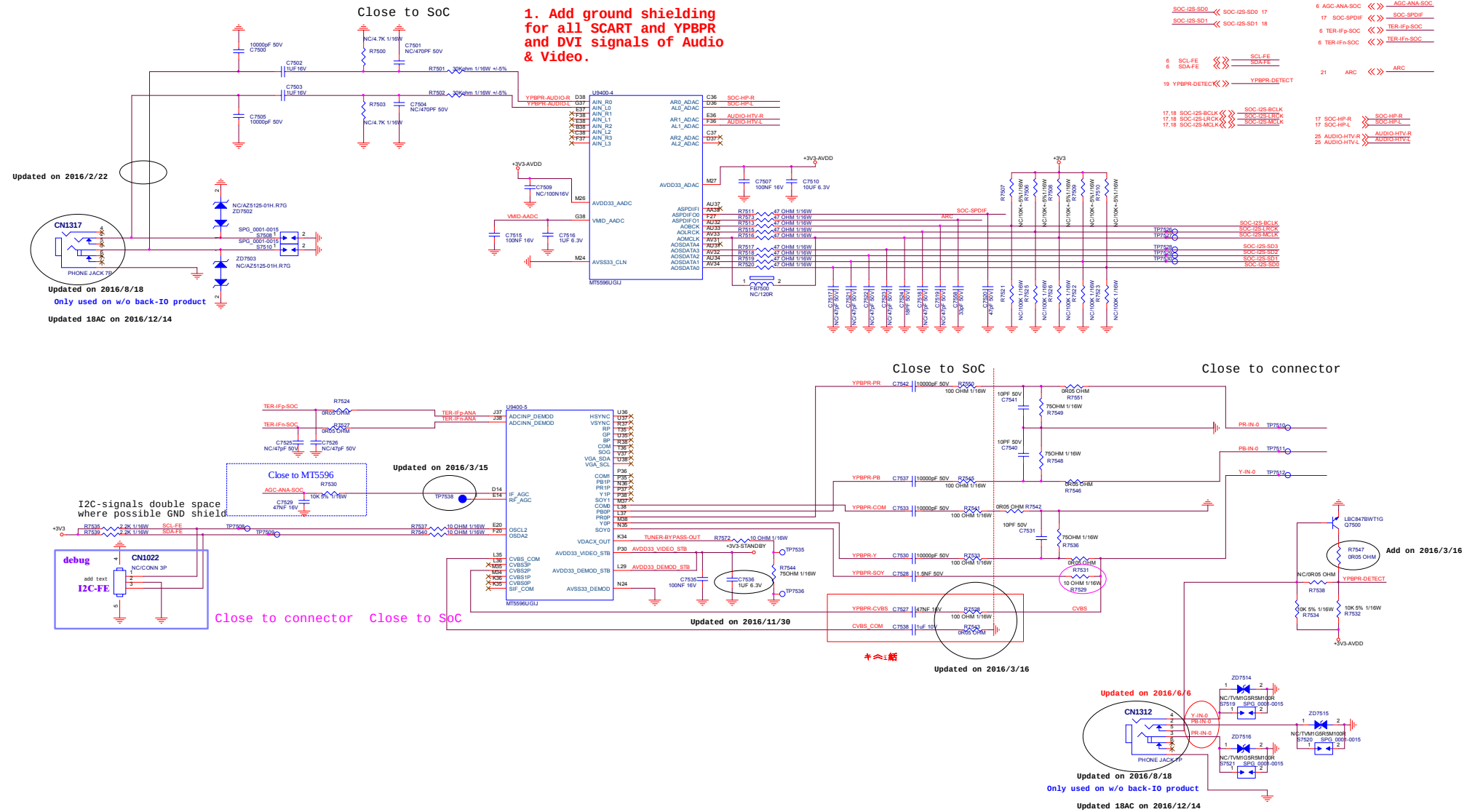


Clearance = 2 x tracewidth for all SCL and SDA

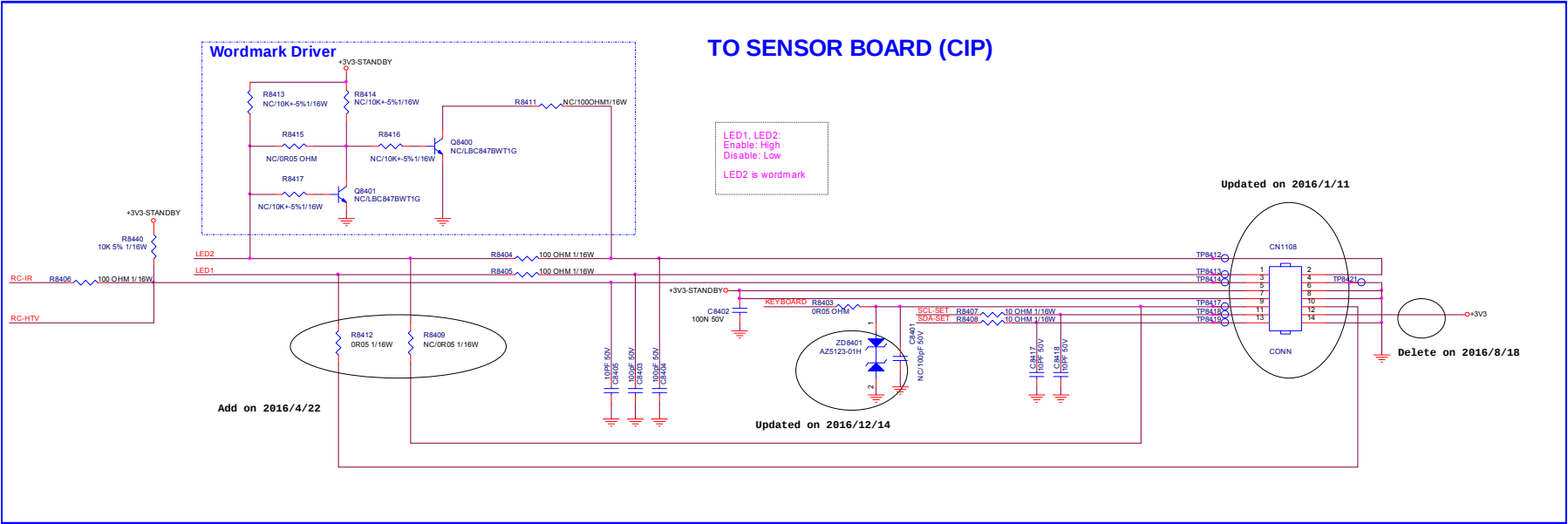
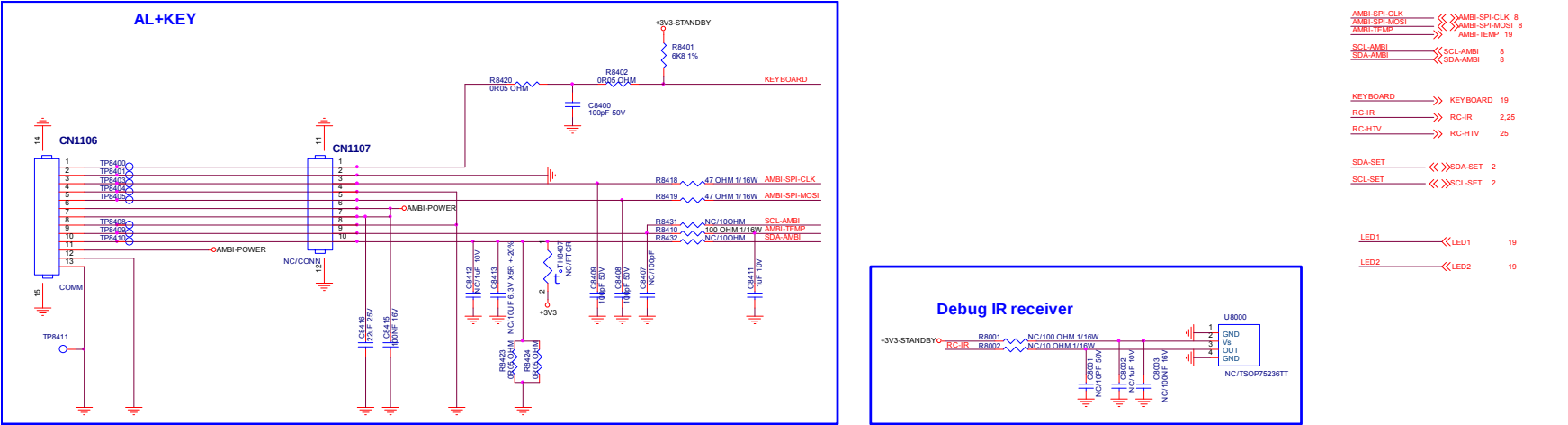


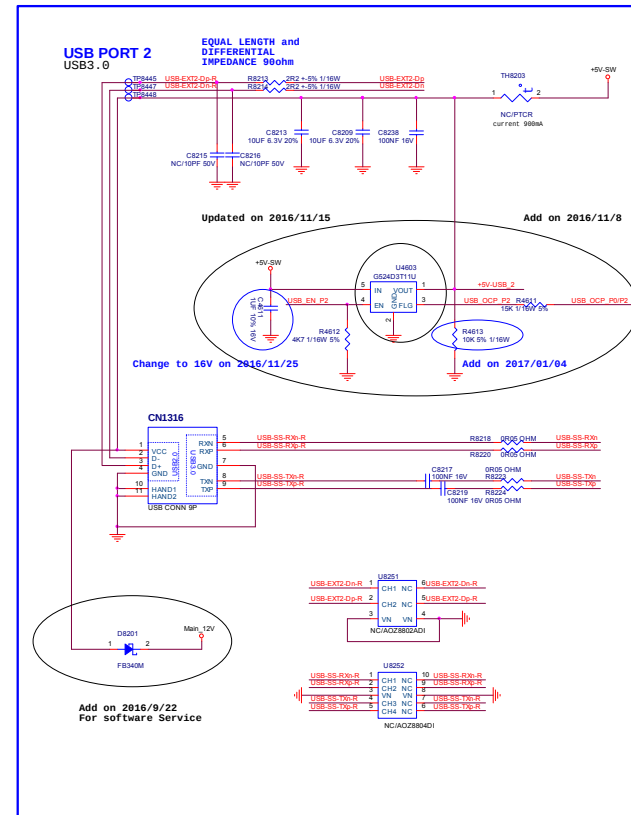
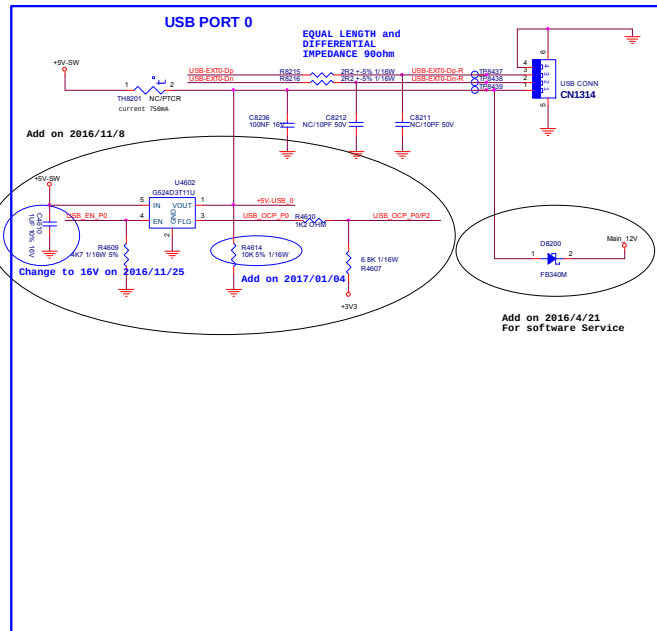
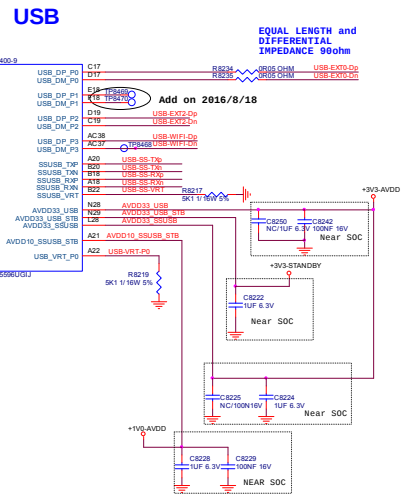
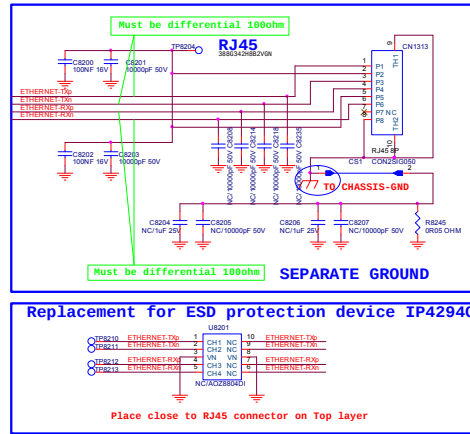
Audio Return Channel (ARC)

8-6-22 SCART-YPbPr-CVBS

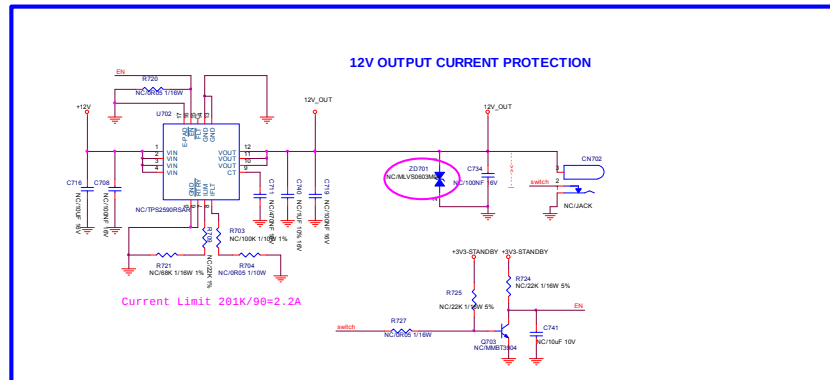
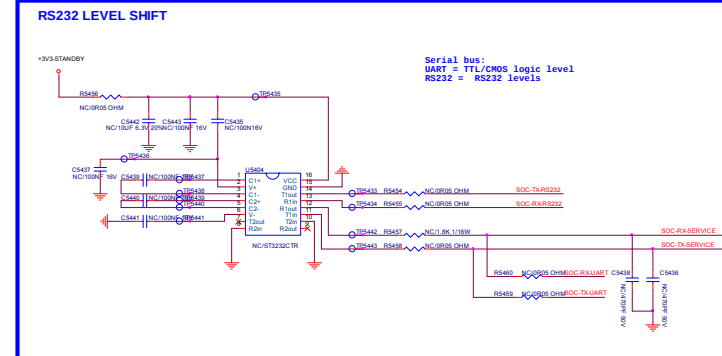
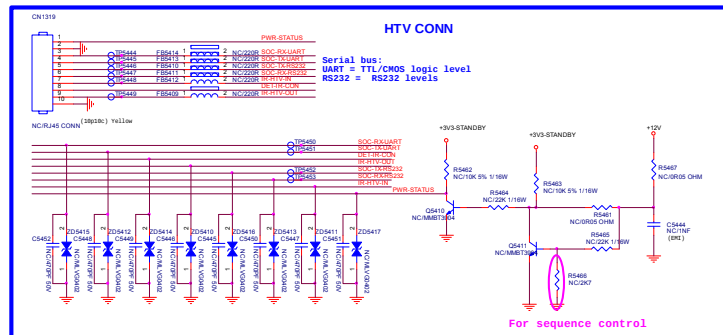
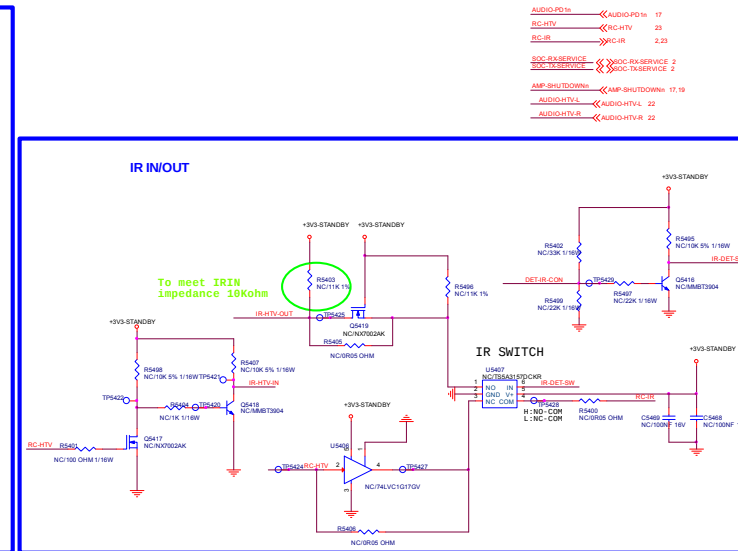
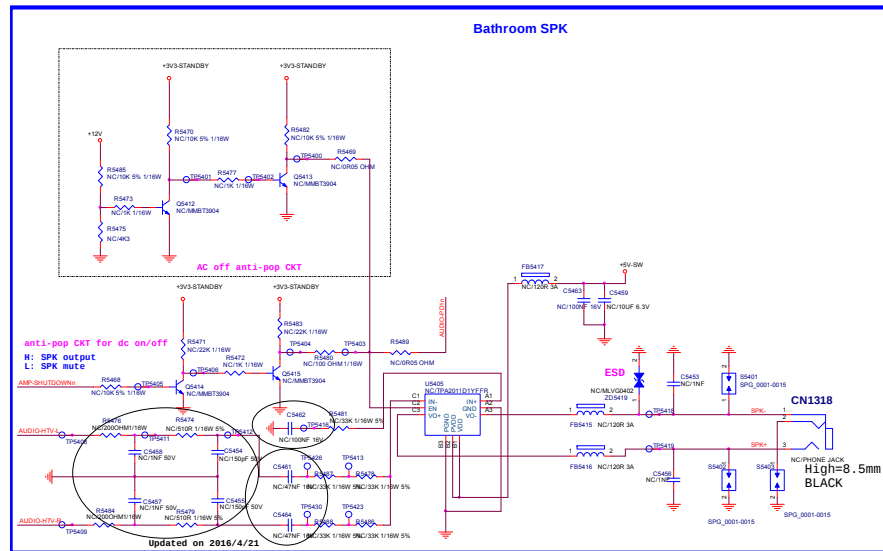


8-6-23 CTRL-CONNECTORS



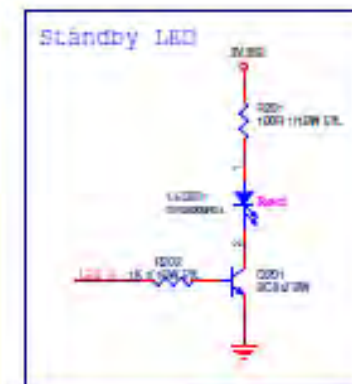
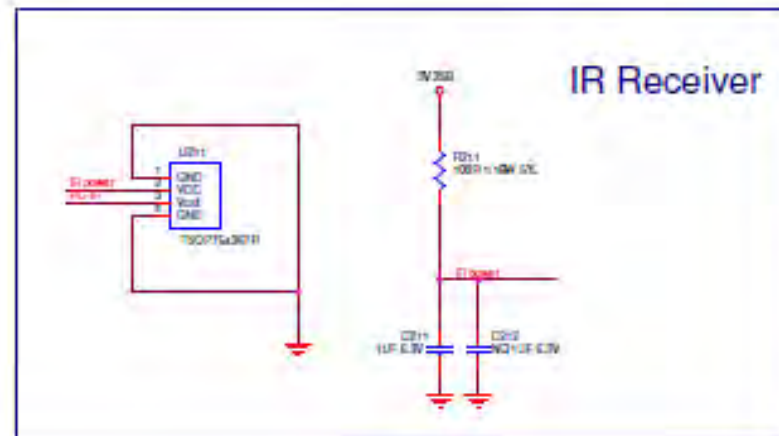
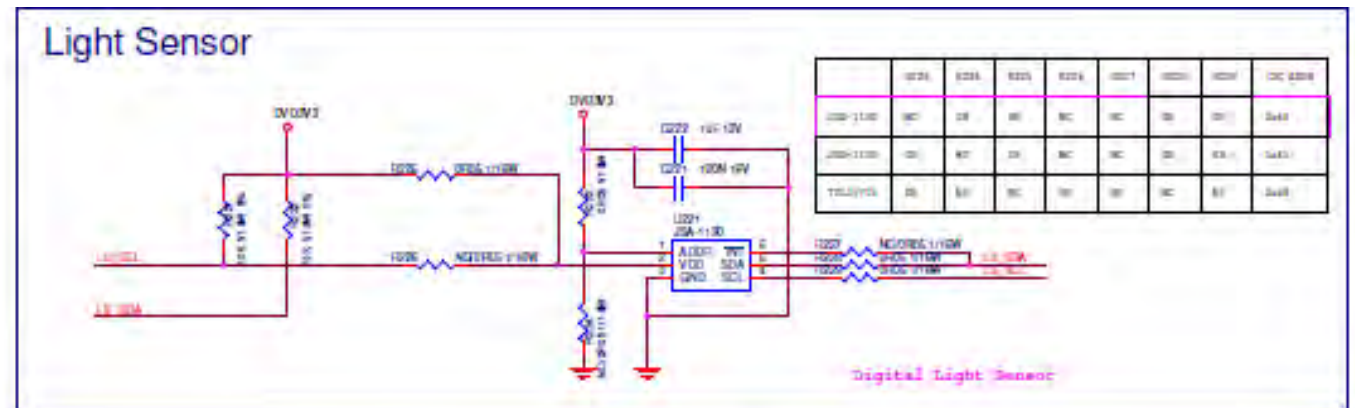
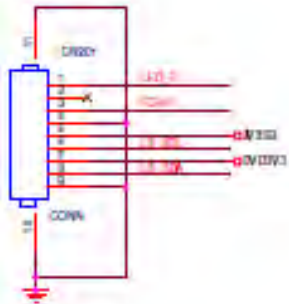
[illegible]

8-6-25 HTV



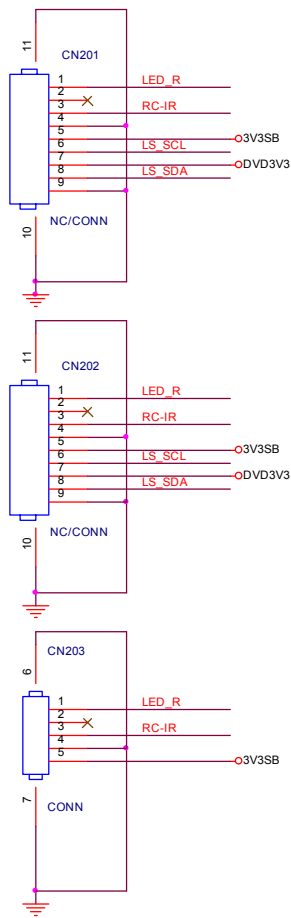
8.7J 715G8694 IR/LED Panel

8-7-1 LED&IR&Light sensor

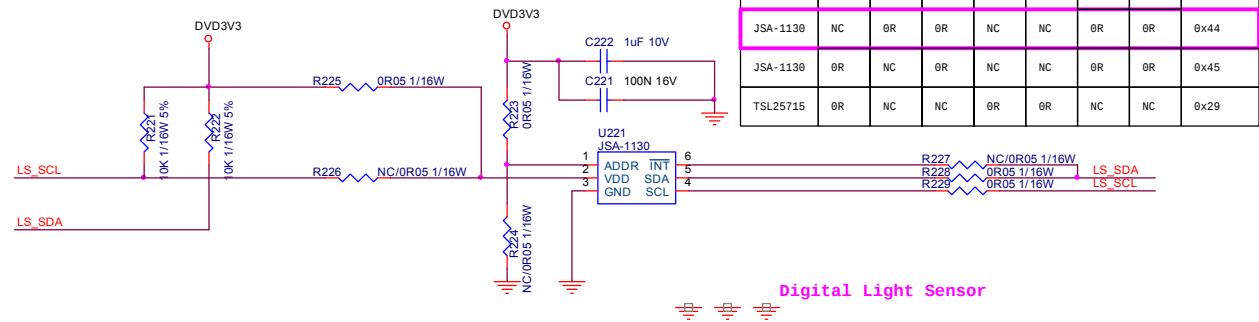


8.8 J 715G8623 IR/LED Panel

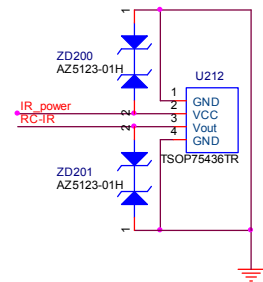
8-8-1 IR



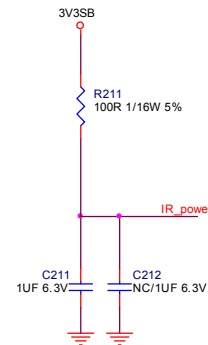
Light Sensor



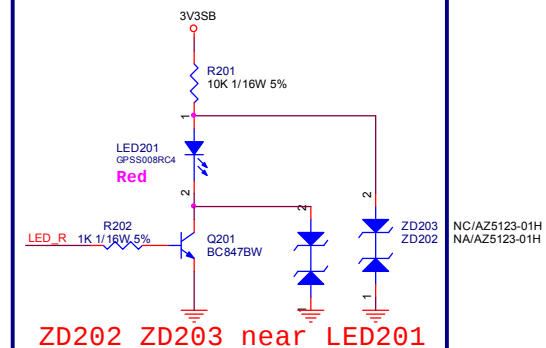
ZD200 ZD201 near U212 pin



IR Receiver

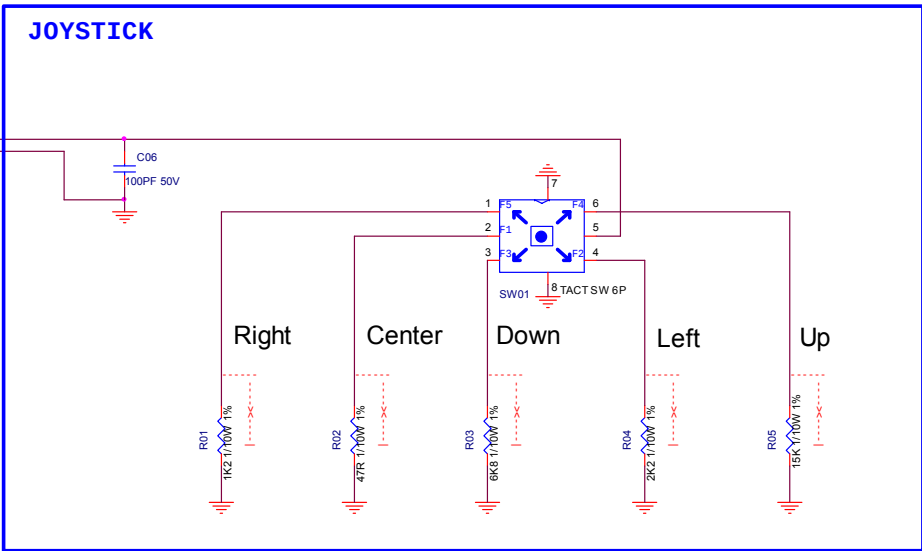
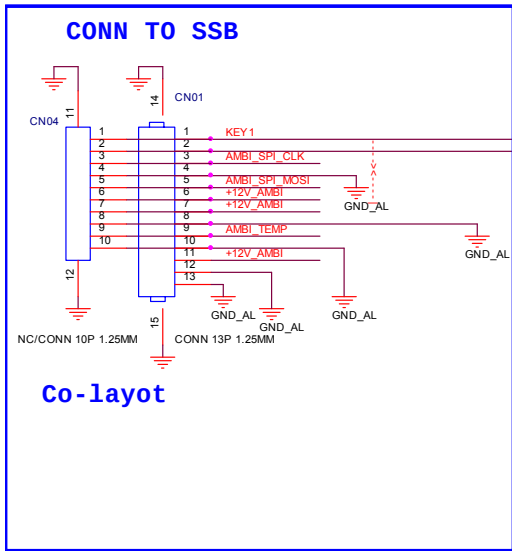


Standby LED



8.9 E 715G8555 Keyboard control panel

8-9-1 Key



Joystick key define

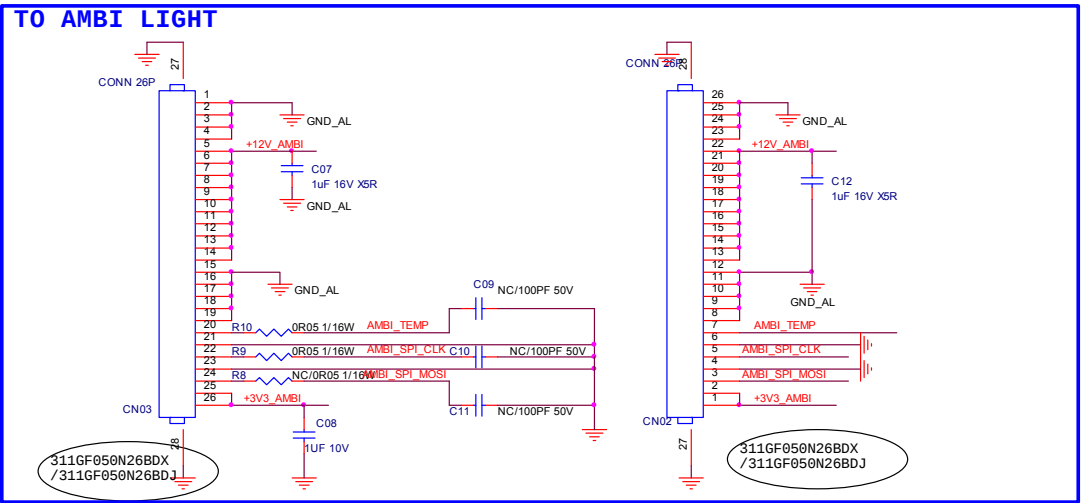
Direction	switch	Key function	Resistance	Voltage	Range
Center	2-5 short	Menu	0R	0V	0.0 to 0.22 V
Right	1-5 short	CH+	1K2	0.5V	0.39 to 0.60 V
Left	4-5 short	CH-	2K2	0.81V	0.67 to 0.95 V
Down	3-5 short	VOL-	6K8	1.65V	1.41 to 1.87 V
Up	6-5 short	VOL+	15K	2.27V	1.93 to 2.58 V
NA	NA	No function	NA	3.3V	3.135 to 3.465V

Joystick circuit diagram

	pin1	pin2	pin3	pin4	pin5	pin6
F1						
F2						
F3						
F4						
F5						

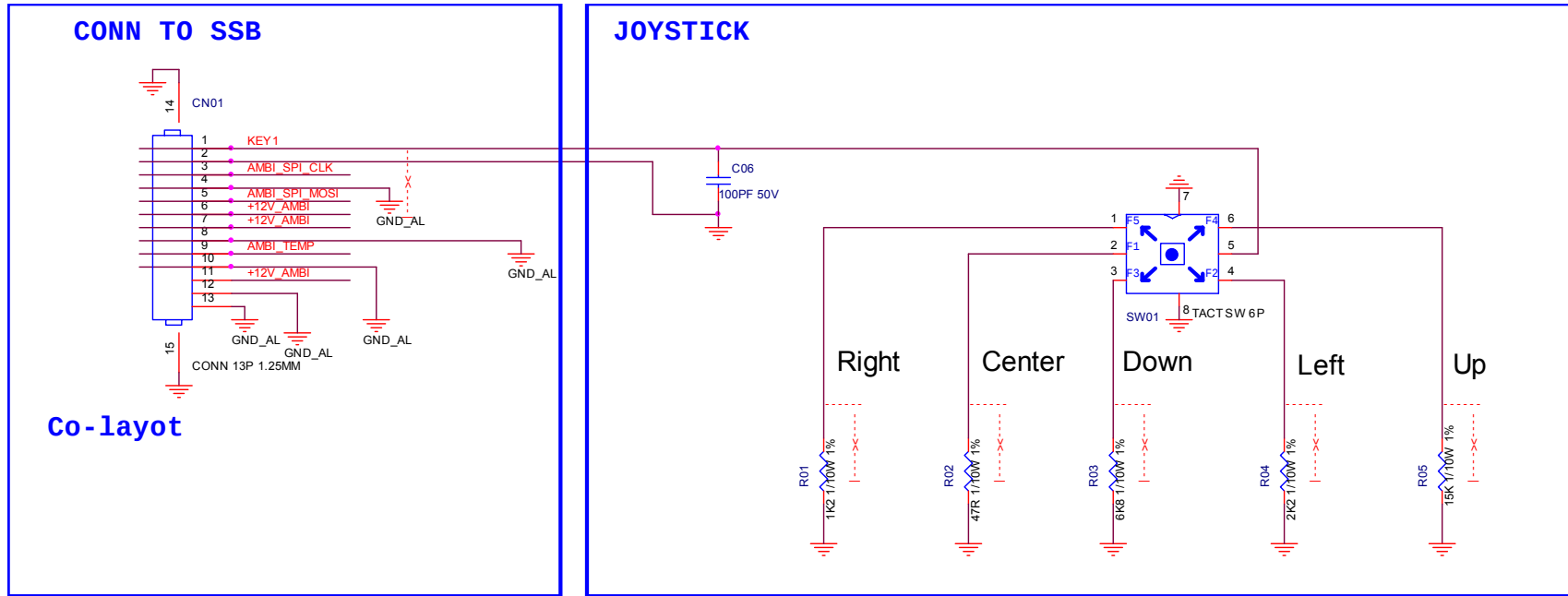
Joystick diversity for AL

	CN03	C07	R9	R10
AL2	N	N	N	N
AL3/AL4	Y	Y	Y	Y



8.10 E 715G7088 Keyboard control panel

8-10-1 Key



TO AMBI LIGHT

